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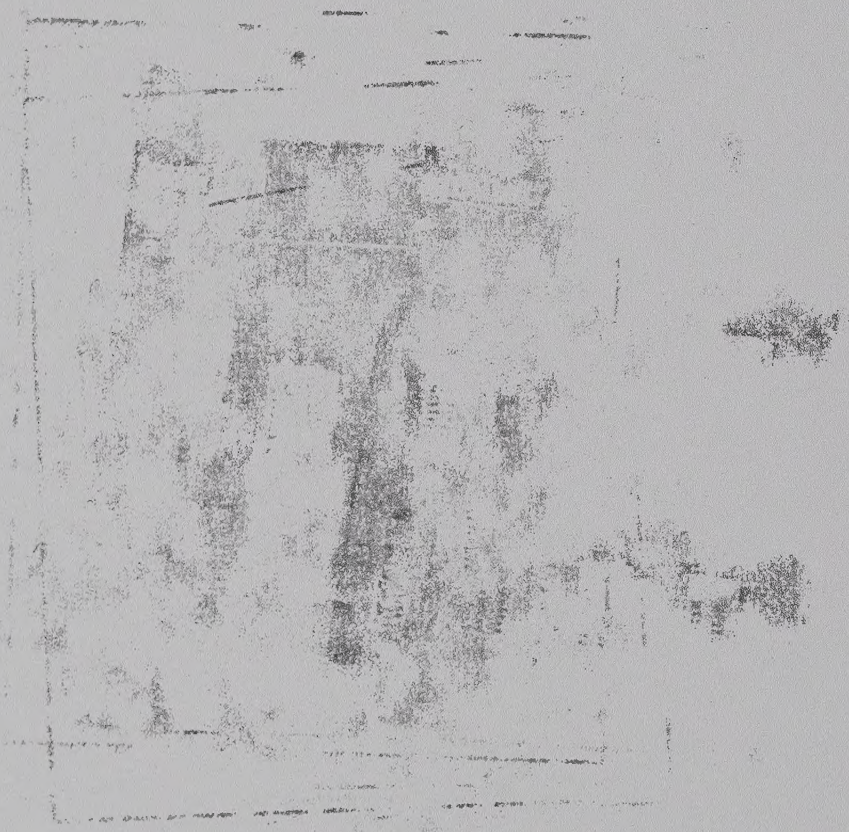

UniPak 2™
950-0059-004

SEPT 83 REV G

10-950-0059

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NOTE

Before using the UniPak 2™, read section 1.2 for programmer mainframe compatibility information.

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SECTION 1
INTRODUCTION

1.1 OVERVIEW

Data I/O's UniPak 2™ reliably programs over 400 popular MOS and bipolar devices. Values for programming variables, including pinouts, voltage levels and timing are stored in firmware tables. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum firmware overhead. The UniPak 2™ is designed to adapt to the programming requirements of many different devices. Pinout variations are handled by seven device sockets on the UniPak 2™ and, in some cases, by adapters which connect to socket 2. Specially designed electronic switches allow programming of both bipolar and MOS devices.

To maximize control speed during programming, the UniPak 2™ makes extensive use of addressable latches for control signals. For flexibility in waveform generation, digital-to-analog converters (DACs) control all major power supplies, with several rise and fall times selected by firmware.

1.2 PROGRAMMER COMPATIBILITY

To be compatible with the UniPak 2™, your programmer may require a hardware and/or firmware update, depending on the model, configuration, and age. The information that follows will help you determine if your programmer requires updating. If you find that your programmer does require updating, contact your nearest Data I/O Service Center.

- System 17—The System 17 must be converted into a System 19 with the latest firmware installed and latest hardware modifications.

- System 19—Check to determine if your System 19 contains a 702-1520 or 702-1980 controller board by performing the following steps.

  1. Remove the programming pak (section 2.3).

  2. Remove the metal shield (if any) shown in figure 2-1.

  3. Count the number of EPROM firmware sockets located just behind the pak interface connector. If there are four sockets, it is a 702-1520 board. If there are eight sockets, it is a 702-1980 board.

If your System 19 contains a 702-1520 controller board check the modification status sticker (figure 1-1) on the bottom of the programmer. If the sticker is not there or if only "1" is marked off, your System 19 requires hardware and firmware updating; contact the nearest Data I/O Service Center. If "2" is marked, your System 19 is compatible with the UniPak 2™. If your System 19 contains a 702-1980 controller board, it may require a firmware update. To display the configuration number of the firmware in your programmer, key in "SELECT-B2-START". If the configuration number displayed matches the number listed below, your firmware needs updating.

MODIFICATION STATUS					
1	2	3	4	5	6
●	0	0	0	0	0

Figure 1-1. Example of A "Modification Status" Sticker

Model	Conf. #
• 990-1902	3599
• 990-1903	CC8B

- 29A Universal Programmer—To be compatible with the UniPak 2™, the 29A programmers must have Rev C or later firmware. To determine the configuration of the firmware in your 29A, key in "SELECT-B2-START" and observe the display. If the hex number matches one listed in table 1-1, your firmware needs to be updated.

- 100A Production Programmer—To be compatible with the UniPak 2™, the 100A programmers must have Rev E or later firmware. To determine the configuration of the firmware in your 100A, key in "SELECT-1Ø" and observe the display. If the hex number displayed matches one listed in table 1-1, your firmware needs to be updated.

Table 1-1. Programmer Compatibility

Model	Rev	Configuration Number
29A	A	1ECA
	B	20A4
29A (with computer remote control)	A	BB41
	B	C00B
100A	A	917F
	B	9405
	C	9DEE
	D	9BED

1.3 APPLICATIONS

Table 1-2 lists all the devices that can be programmed with the UniPak 2™ at the time this manual was published. In many cases when a new device with industry-standard pinout is introduced within a manufacturer's family, the UniPak 2™ WILL NOT require a revision to program it. For some new applications, such as to accommodate a new device family, a firmware update of the UniPak 2™ may be required. The revision number is stamped after the part number (950-0059) along the underside of the top edge of the UniPak 2™ socket assembly.

1.4 SPECIFICATIONS

The UniPak 2™ receives its power from the programmer mainframe. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling firmware is located on a circuit card within the UniPak 2™.

The physical and environmental specifications are:

Altitude: Sea level to 3 km (10,000ft)

Dimensions: 20.9 x 17.0 x 10.5cm (8.2 x 6.7 x 4.2in.)

Humidity (operating): 90% maximum (non condensing)

Humidity (storage): 95% maximum (non condensing)

Temperature (operating): 0 to 40°C (32 to 104°F)

Temperature (storage): −40 to 55°C (−40 to 131°F)

Weight: 1.38kg (3lb, 0.5oz)

1.5 FIELD APPLICATION SUPPORT

Data I/O has field applications engineers (FAE's) throughout the world. They can provide additional information about interfacing Data I/O products with other equipment and answer questions about equipment. FAE's are located within the United States at the address listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of 90 days begins when you receive the equipment. The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O service center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. In addition to repairs, all Data I/O products can be calibrated at service centers. A list of all Data I/O service centers is located in the back of this manual.

1.8 ORDERING

To order equipment, contact your Data I/O sales representative. Orders must contain the following information:

- description of the equipment (See the latest Data I/O price list or contact your sales representative for equipment and part numbers.),
- quantity of each item ordered,
- shipping and billing address of firm, including zip code,
- name of person ordering equipment,
- purchase order number,
- desired method of shipment.

Table 1-2. UniPak 2™ Family and Pinout Codes

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Advanced Micro Devices						
27LS18	16	02	V03	-	A	
27LS19	16	02	V03	-	A	
27S18	16	02	V03	-	A	
27S19	16	02	V03	-	A	
29750A	16	02	V03	-	O	
29751A	16	02	V03	-	O	
27S20	16	01	V03	-	A	
27S21	16	01	V03	-	A	
29760A	16	01	V03	-	O	
29761A	16	01	V03	-	O	
27S12	16	03	V03	-	A	
27S13	16	03	V03	-	A	
29770	16	03	V03	-	O	
29771	16	03	V03	-	O	
27S15	16	79	V04	351A-068	A	
27S24	16	65	V03	-	A	
27S25	16	65	V03	-	A	
27S26	16	85	V04	351A-067	A	
27S27	16	85	V04	351A-067	A	
27S28	16	09	V03	-	A	
27S29	16	09	V03	-	A	
27S30	16	36	V03	-	A	
27S31	16	36	V03	-	A	
29774	16	85	V04	351A-067	S	
29775	16	85	V04	351A-067	S	
27S32	16	38	V03	-	A	
27S33	16	38	V03	-	A	
27PS181	16	37	V03	-	A	
27PS281	16	37	V03	-	A	
27S180	16	37	V03	-	A	
27S181	16	37	V03	-	A	
27S280	16	37	V03	-	A	
27S281	16	37	V03	-	A	
27S35	16	66	V03	-	A	
27S37	16	66	V03	-	A	
27PS184	16	06	V03	-	A	
27PS185	16	06	V03	-	A	
27S184	16	06	V03	-	A	
27S185	16	06	V03	-	A	
27PS191	16	68	V03	-	A	
27PS291	16	68	V03	-	A	
27S190	16	68	V03	-	A	
27S191	16	68	V03	-	A	
27S290	16	68	V03	-	A	
27S291	16	68	V03	-	A	
27S45	16	77	V04	351A-066	A	
27S47	16	77	V04	351A-066	A	
27PS41	16	53	V03	-	A	
27S40	16	53	V03	-	A	
27S41	16	53	V03	-	A	
27PS43	16	63	V03	-	A	
27S43	16	63	V03	-	A	
27PS49	16	67	V03	-	A	
27S49	16	67	V03	-	A	
2708	21	27	V03	-	A	
AM9708	21	27	V03	-	A	
2716	19	23	V03	-	A	
AM9716	19	23	V03	-	A	
2732	19	24	V03	-	A	
2732A	27	24	V03	-	A	
AM9732	19	24	V03	-	A	
2764	AF	33	V04	-	A	
AM9764	AF	33	V04	-	A	
27128	AF	51	V04	-	A	
Electronic Arrays						
2708	21	27	V03	-	S	
2716	19	23	V03	-	S	
Fairchild						
93417	01	01	V03	-	A	
93427	01	01	V03	-	A	
93436	01	03	V03	-	A	
93446	01	03	V03	-	A	
93438	01	15	V03	-	A	
93448	01	15	V03	-	A	
93452	01	05	V03	-	A	
93453	01	05	V03	-	A	
93450	01	16	V03	-	A	
93451	01	16	V03	-	A	
93460	01	16	V03	-	A	
93461	01	16	V03	-	A	
93L450	01	16	V03	-	A	
93L451	01	16	V03	-	A	
93510	01	21	V03	-	A	
93511	01	21	V03	-	A	
93Z450	A4	16	V04	-	A	
93Z451	A4	16	V04	-	A	
93Z510	A4	21	V04	-	A	
93Z511	A4	21	V04	-	A	
93Z512	A4	53	V04	-	S	
93Z513	A4	53	V04	-	S	
93Z564	A4	67	V04	-	S	
93Z565	A4	67	V04	-	S	
2708	21	27	V03	-	A	
Fujitsu						
27C64	45	33	V04	-	S	
27C128	45	51	V04	-	S	
7051	78	02	V03	-	A	
7056	78	02	V03	-	A	
7111	68	02	V03	-	A	
7112	68	02	V03	-	A	
7052	78	01	V03	-	A	
7057	78	01	V03	-	A	
7113	68	01	V03	-	A	
7114	68	01	V03	-	A	
7117	68	08	V03	-	A	
7118	68	08	V03	-	A	
7119	68	14	V03	-	A	
7120	68	14	V03	-	A	
7053	78	03	V03	-	A	
7058	78	03	V03	-	A	
7115	68	03	V03	-	A	
7116	68	03	V03	-	A	
7123	68	09	V03	-	A	
7124	68	09	V03	-	A	
7125	68	15	V03	-	A	
7126	68	15	V03	-	A	
7054	78	05	V03	-	A	
7059	78	05	V03	-	A	
7121	68	05	V03	-	A	
7122	68	05	V03	-	A	
7055	78	69	V03	-	A	
7060	78	69	V03	-	A	
7131	68	16	V03	-	A	
7132	68	16	V03	-	A	
7127	68	06	V03	-	A	
7128	68	06	V03	-	A	
7137	68	21	V03	-	A	
7138	68	21	V03	-	A	
7133	68	11	V03	-	A	
7134	68	11	V03	-	A	
7141	68	63	V03	-	A	
7142	68	63	V03	-	A	
7143	68	67	V03	-	A	
7144	68	67	V03	-	A	
8518	21	27	V03	-	S	
8516	19	23	V03	-	S	
8742	50	57	V04	351A-070	S	
8749H	50	57	V04	351A-070	S	
2732A	27	24	V03	-	-	
2732A-35	27	24	V03	-	S	
27C32A	27	24	V03	-	S	
8532	19	24	V03	-	S	
2764	45	33	V04	-	S	
27128	45	51	V04	-	S	
General Instruments						
5716	83	23	V03	-	A	
5816	37	23	V03	-	A	
Harris						
6641	40	47	V03	-	A	
7602	05	02	V04	-	A	
7603	05	02	V04	-	A	
7610	05	01	V03	-	A	
7611	05	01	V03	-	A	
7620	05	03	V03	-	A	
7621	05	03	V03	-	A	
7640	05	15	V03	-	A	
7641	05	15	V03	-	A	
7648	05	09	V03	-	A	
7649	05	09	V03	-	A	
7642	05	05	V03	-	A	
7643	05	05	V03	-	A	

Table 1-2. UniPak 2™ Family and Pinout Codes (continued)

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Harris (continued)						
7608	05	16	V03	-	A	
7680	05	16	V03	-	A	
7681	05	16	V03	-	A	
7684	05	06	V03	-	A	
7685	05	06	V03	-	A	
7616	05	42	V03	-	A	
76161	05	21	V03	-	A	
76165	05	53	V03	-	A	
76321	05	63	V03	-	A	
76641	05	67	V03	-	A	
Hitachi						
25044	74	05	V03	-	A	
25045	74	05	V03	-	A	
25088	74	16	V03	-	A	
25089	74	16	V03	-	A	
25084	74	06	V03	-	A	
25085	74	06	V03	-	A	
25168	74	21	V03	-	A	
25169	74	21	V03	-	A	
27C32A	27	24	V03	-	A	
462716	19	23	V03	-	S	
48016	33	23	V03	-	S	
462532	19	25	V03	-	S	
462732	19	24	V03		S	
462732P	19	24	V03	-	S	
482732A	27	24	V03		S	
482764	79	33	V03	-	S	
4827128	79	51	V03	-	S	
Hughes						
3004-1	58	62	V04	-	S	
3004-2	58	61	V04	-	S	
3704-1	58	62	V04	-	S	
3704-2	58	61	V04	-	S	
3008	58	60	V04	-	S	
3708	58	60	V04	-	S	
Intel						
3628	75	16	V03	-	A	
3628A	75	16	V03	-	A	
82HS181	75	16	V03	-	A	
82S181	75	16	V03	-	A	
3636	75	21	V03	-	A	
3636B	75	21	V03	-	A	
82HS191	75	21	V03	-	A	
82S191	75	21	V03	-	A	
3632	75	63	V03	-	A	
82HS321	75	63	V03	-	A	
82S321	75	63	V03	-	A	
2704	21	26	V03	-	A	
8704	21	26	V03	-	A	
2708	21	27	V03	-	A	
2758	19	22	V03	-	A	
8708	21	27	V03	-	A	
8741	56	59	V04	351A-070	S	
8748	52	56	V04	351A-070	S	
8748H	50	56	V04	351A-070	S	
2716	19	23	V03	-	A	
2815	85	23	V03	-	A	
2816	37	23	V03	-	A	
8742	50	57	V04	351A-070	S	
8749H	50	57	V04	351A-070	S	
8755A	47	55	V04	351A-072	S	
2732	19	24	V03	-	A	
2732A	27	24	V03	-	A	
8751	53	58	V04	351A-071	S	
2764	79	33	V03	-	A	
27128	79	51	V03	-	A	
27256	93	32	V04	-	A	
Intersil						
5600	70	02	V03	-	A	
5610	70	02	V03	-	A	
5603A	70	01	V03	-	A	
5623	70	01	V03	-	A	
5604	70	03	V03	-	A	
5624	70	03	V03	-	A	
6716	59	64	V03	-	A	
Mitsubishi						
2708	21	27	V03	-	S	
58732S	21	27	V03	-	S	

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Mitsubishi (continued)						
2716	19	23	V03	-	S	
2732	19	24	V03	-	S	
2764	79	33	V03		S	
27128	79	51	V03	-	S	
Monolithic Memories						
5330	29	02	V03	-	A	
5331	29	02	V03	-	A	
6330	29	02	V03	-	A	
6331	29	02	V03	-	A	
63LS080	18	02	V03	-	A	
63LS081	18	02	V03	-	A	
63S080	18	02	V03	-	A	
63S081	18	02	V03	-	A	
5300	11	01	V03	-	A	
5301	11	01	V03	-	A	
5300	11	01	V03	-	A	
6301	11	01	V03	-	A	
63LS140	18	01	V03	-	A	
63LS141	18	01	V03	-	A	
63S140	18	01	V03	-	A	
63S141	18	01	V03	-	A	
5308	11	08	V03	-	A	
5309	11	08	V03	-	A	
5335	11	14	V03	-	A	
5336	11	14	V03	-	A	
6308	11	08	V03		A	
6309	11	08	V03	-	A	
6335	11	14	V03	-	A	
6336	11	14	V03	-	A	
5305	11	03	V03	-	A	
5306	11	03	V03	-	A	
6305	11	03	V03	-	A	
6306	11	03	V03	-	A	
63LS240	18	03	V03	-	A	
63LS241	18	03	V03	-	A	
63S240	18	03	V03	-	A	
63S241	18	03	V03	-	A	
5340	11	15	V03	-	A	
5340JS	11	15	V03	-	A	
5341	11	15	V03	-	A	
5341JS	11	15	V03	-	A	
5348	11	09	V03	-	A	
5349	11	09	V03	-	A	
6340	11	15	V03	-	A	
6340JS	11	15	V03	-	A	
6341	11	15	V03	-	A	
6341JS	11	15	V03	-	A	
6348	11	09	V03	-	A	
6349	11	09	V03	-	A	
63S480	18	09	V03	-	A	
63S481	18	09	V03	-	A	
5352	11	05	V03	-	A	
5353	11	05	V03	-	A	
6352	11	05	V03	-	A	
6353	11	05	V03	-	A	
63RS441	18	07	V03	-	A	
63S440	18	05	V03	-	A	
63S441	18	05	V03	-	A	
5380	11	16	V03	-	A	
5380JS	11	16	V03	-	A	
5381	11	16	V03	-	A	
5381JS	11	16	V03	-	A	
6380	11	16	V03	-	A	
6380JS	11	16	V03	-	A	
6381	11	16	V03	-	A	
6381JS	11	16	V03	-	A	
63RS881	18	86	V04	-	A	
5388	11	06	V03	-	A	
5389	11	06	V03	-	A	
6388	11	06	V03	-	A	
6389	11	06	V03	-	A	
63RA841	18	11	V03	-	A	
63S840	18	06	V03	-	A	
63S841	18	06	V03	-	A	
63PL1681	18	21	V03	-	S	
63PS1681	18	21	V03	-	S	
63S1680	18	21	V03	-	A	
63S1681	18	21	V03	-	A	
63S1640	18	53	V03	-	A	
63S1641	18	53	V03	-	A	
63S3281	18	63	V03	-	A	

Table 1-2. UniPak 2™ Family and Pinout Codes (continued)

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Mostek						
2716	19	23	V03	-	A	
Motorola						
7620	05	03	V03	-	A	
7621	05	03	V03	-	A	
7640	05	15	V03	-	A	
7641	05	15	V03	-	A	
7649	05	09	V03	-	A	
7642	05	05	V03	-	A	
7643	05	05	V03	-	A	
7680	05	16	V03	-	A	
7681	05	16	V03	-	A	
7684	05	06	V03	-	A	
7685	05	06	V03	-	A	
76161	05	21	V03	-	A	
76165	05	53	V03	-	S	
MCM2808	81	72	V03	-	A	
MCM68708	21	27	V03	-	A	
MCM2716	19	23	V03	-	A	
MCM2816	43	23	V03	-	A	
MCM2817	81	71	V03	-	A	
TMS2716	23	28	V03	-	A	
MCM2532	19	25	V03	-	A	
MCM2832	81	70	V03	-	A	
MCM68764	25	29	V03	-	A	
MCM68766	25	29	V03	-	A	
National Semiconductor						
27C16	19	23	V03	-	A	
25C32	19	25	V03	-	A	
27C32	19	24	V03	-	A	
74S188	08	02	V03	-	A	
74S288	08	02	V03	-	A	
74S287	08	01	V03	-	A	
74S387	08	01	V03	-	A	
74LS471	08	08	V03	-	A	
74S471	08	08	V03	-	A	
74S570	08	03	V03	-	A	
74S571	08	03	V03	-	A	
74S472	08	09	V03	-	A	
74S473	08	09	V03	-	A	
74S474	08	15	V03	-	A	
74S475	08	15	V03	-	A	
87S295	08	15	V03	-	A	
87S296	08	15	V03	-	A	
74S572	08	05	V03	-	A	
74S573	08	05	V03	-	A	
74S574	08	34	V03	-	A	
87LS181	08	16	V03	-	A	
87S180	08	16	V03	-	A	
87S280	08	16	V03	-	A	
87S281	08	16	V03	-	A	
87S184	08	06	V03	-	A	
87S185	08	06	V03	-	A	
87S190	08	21	V03	-	A	
87S191	08	21	V03	-	A	
87S290	08	21	V03	-	A	
87S291	08	21	V03	-	A	
87S195	08	53	V03	-	A	
87S321	08	63	V03	-	A	
2708	21	27	V03	-	A	
2758A	19	22	V03	-	A	
2758B	19	35	V03	-	A	
2716	19	23	V03	-	A	
2816	37	23	V03	-	A	
9716	B3	23	V04	-	A	
2532	19	25	V03	-	A	
2732	19	24	V03	-	A	
2764	35	33	V03	-	S	
Nippon Electronic Company, Ltd.						
B403	72	01	V03	-	A	
B423	72	01	V03	-	A	
B405	72	15	V03	-	A	
B425	72	15	V03	-	A	
B406	72	05	V03	-	A	
B426	72	05	V03	-	A	
B408	72	16	V03	-	A	
B417	72	16	V03	-	A	
B428	72	16	V03	-	A	
B409	72	21	V03	-	A	
B419	72	42	V03	-	A	

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Nippon Electronic Company, Ltd. (continued)						
B429	72	21	V03	-	A	
8741AD	56	59	V04	351A-070	S	
8748AD	52	56	V04	351A-070	S	
2716	19	23	V03	-	A	
8755A	47	55	V04	351A-072	S	
2732	19	24	V03	-	A	
2732A	27	24	V03	-	A	
2764	79	33	V03	-	A	
Oki						
2708	21	27	V03	-	S	
2758	19	22	V03	-	S	
2716	19	23	V03	-	S	
8755A	47	55	V04	351A-072	S	
2732A	27	24	V03	-	S	
2764	79	33	V03	-	S	
27128	79	51	V03	-	S	
Raytheon						
29660	11	01	V03	-	A	
29661	11	01	V03	-	A	
29662	11	01	V03	-	A	
29663	11	01	V03	-	A	
29600	11	08	V03	-	A	
29601	11	08	V03	-	A	
29602	11	08	V03	-	A	
29603	11	08	V03	-	A	
29610	11	03	V03	-	A	
29611	11	03	V03	-	A	
29612	11	03	V03	-	A	
29613	11	03	V03	-	A	
29620	11	09	V03	-	A	
29621	11	09	V03	-	A	
29622	11	09	V03	-	A	
29623	11	09	V03	-	A	
29624	11	15	V03	-	A	
29625	11	15	V03	-	A	
29626	11	15	V03	-	A	
29627	11	15	V03	-	A	
29630	11	16	V03	-	A	
29630SM	11	16	V03	-	A	
29631	11	16	V03	-	A	
29631SM	11	16	V03	-	A	
Raytheon						
29632	11	16	V03	-	A	
29632SM	11	16	V03	-	A	
29633	11	16	V03	-	A	
29633SM	11	16	V03	-	A	
29634	11	16	V03	-	A	
29635	11	16	V03	-	A	
29636	11	16	V03	-	A	
29637	11	16	V03	-	A	
29650	11	06	V03	-	A	
29651	11	06	V03	-	A	
29652	11	06	V03	-	A	
29653	11	06	V03	-	A	
29680	11	21	V03	-	A	
29680SM	11	21	V03	-	A	
29681	11	21	V03	-	A	
29681SM	11	21	V03	-	A	
29682	11	21	V03	-	A	
29682SM	11	21	V03	-	A	
29683	11	21	V03	-	A	
29683SM	11	21	V03	-	A	
29640	11	53	V03	-	A	
29641	11	53	V03	-	A	
29642	11	53	V03	-	A	
29643	11	53	V03	-	A	
29671	11	63	V03	-	A	
29673	11	63	V03	-	A	
Ricoh						
RD5H32	27	24	V03	-	S	
Seeq						
5213	A5	96	V04	-	A	
5213H	A5	96	004	-	A	
52B13	A5	96	004	-	A	
52B13H	A5	96	004	-	A	
5133	35	33	V03	-	A	
5133H	79	33	V03	-	A	
5143	79	51	V03	-	A	

Table 1-2. UniPak 2™ Family and Pinout Codes (continued)

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
SGS Technology						
2716	19	23	V03	-	A	
2732	19	24	V03	-	A	
Signetics						
82123	10	02	V03	-	A	
82S123	10	02	V03	-	A	
82S23	10	02	V03	-	A	
82S126	10	01	V03	-	A	
82S129	10	01	V03	-	A	
82S114	AE	84	V04	351A-068	S	
82S135	10	08	003	-	A	
82S130	10	03	003	-	A	
82S131	10	03	003	-	A	
82S115	AE	83	V04	351A-068	S	
82S140	10	15	003	-	A	
82S141	10	15	003	-	A	
82S146	10	09	003	-	A	
82S147	10	09	003	-	A	
82LS137	10	05	003	-	A	
82S138	10	05	003	-	A	
82S137	10	05	003	-	A	
82LS180	10	16	003	-	A	
82LS181	10	16	003	-	A	
82PS180	10	16	003	-	A	
82PS181	10	16	003	-	A	
82S180	10	16	003	-	A	
82S181	10	16	003	-	A	
82S182	10	16	003	-	A	
82S183	10	16	003	-	A	
82S2708	10	16	003	-	A	
82S184	10	06	003	-	A	
82S185	10	06	003	-	A	
82S190	10	21	003	-	A	
82S191	10	21	003	-	A	
82S195	10	53	003	-	A	
82S321	10	63	003	-	A	
2708	21	27	003	-	A	
Synertek						
2716	19	23	003	-	A	
Thompson						
71190	92	21	003	-	S	
71191	92	21	003		S	
Texas Instruments						
24S10	13	01	003	-	A	
24SA10	13	01	003	-	A	
28L22	13	46	003		A	
28LA22	13	46	003	-	A	

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Texas Instruments (continued)						
28L42	13	09	003	-	A	
28L45	13	15	003	-	A	
28P42	13	09	003	-	A	
28P45	13	15	003	-	A	
28S42	13	09	003	-	A	
28S45	13	15	003	-	S	
28S46	13	15	003	-	A	
28SA42	13	09	003	-	A	
28SA46	13	15	003	-	A	
24S41	13	38	V03	-	A	
24SA41	13	38	V03	-	A	
28L85	13	16	V03	-	A	
28L86	13	16	V03	-	A	
28P85	13	16	V03	-	A	
28S2708	13	16	V03	-	A	
28S85	13	16	V03	-	S	
28S86	13	16	V03	-	A	
28SA86	13	16	V03	-	A	
24S81	13	06	V03	-	A	
24SA81	13	06	V03	-	A	
28L166	13	21	V03	-	A	
28P166	13	21	V03	-	A	
28S166	13	21	V03	-	A	
28SA166	13	21	V03	-	A	
24S166	13	53	V03	-	A	
24SA166	13	53	V03	-	A	
2508	19	22	V03		A	
2708	21	27	V03	-	A	
27L08	21	27	V03	-	A	
2516	31	23	V04	-	A	
TMS2716	23	28	V03		A	
2532	19	25	V03	-	A	
2732	31	24	V03	-	A	
2732A	27	24	V03	-	A	
2564	31	30	V03	-	A	
2764	35	33	V03		A	
27128	35	51	V03	-	S	
Toshiba						
321	21	26	V03	-	S	
322	21	27	V03	-	S	
323	19	23	V03	-	S	
8755AC	47	55	V04	351A-072	S	
2732	19	24	V03	-	S	
2764	79	33	V03	-	S	
27128	79	51	V03	-	S	
Xicor						
2804	37	82	V04	-	A	
2816	37	23	V04	-	A	

KEY TO HEADINGS AND FOOTNOTES

- **Device Part Number.** The number assigned by the device manufacturer.
- **Family Code.** A 2-digit number that designates the programming algorithm.
- **Pinout Code.** A 2-digit number used to differentiate device types based on pin assignment and array size.
- **UniPak 2™ Software Version.** A number in this column specifies the earliest software version of the UniPak 2™ that will program the device to the manufacturer's latest specifications.
- **Socket Adapter.** Model number of the socket adapter that programs the device. If a number does not appear in this column, use the lighted front panel socket to program your device.
- **Notes.** The following is an explanation of the letters that appear in the Notes column.

  O - This device is obsolete and no longer in production.

  A - This device is currently in production. Data I/O has a written manufacturer approval for this device's programming algorithm.

  S - Programming algorithm for this device is installed within the programmer; manufacturer approval has been requested.

SECTION 2
INSTALLATION

2.1 INSPECTION

The UniPak 2™ was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should, therefore, arrive free of any defect, without marks or scratches, and in perfect operating condition. Carefully inspect the instrument for any damage that may have occurred in transit; if you note any damage, file a claim with the carrier and notify Data I/O.

2.2 UNIPAK 2™ INSTALLATION

The UniPak 2™ may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the UniPak 2™ is installed, you will hear a "beep" until the UniPak 2™ is installed.

NOTE

Voltage transients can cause device damage. Be sure that all sockets are empty when:

- *switching power on or off*

or

- *installing or removing the UniPak 2™*

To install the UniPak 2™, do the following:

1. Slide the UniPak 2™ into the opening in the programmer (figure 2-1).

2. Tilt the UniPak 2™ up and gently push it back to hook the flange of the UniPak 2™ over the back edge of the programmer opening (figure 2-1, a).

3. Lower the UniPak 2™ into position as shown in figure 2-1, b.

4. Press gently on the front edge of the UniPak 2™ to ensure a good connection (figure 2-1, c).

2.3 UNIPAK 2™ REMOVAL

1. Check to make sure the programmer is not in the middle of an operation. If it is, wait until the operation is complete (the action symbol on the display disappears).

2. Check to make sure a device is not in a socket. If one is in a socket, remove it as described in section 3.7.

3. Tilt the UniPak 2™ up and gently remove it from the programmer.

2.4 REPACKING FOR SHIPMENT

If the UniPak 2™ is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and name. If the original shipping container is to be used, place the UniPak 2™ in the container with the appropriate packing material and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE".

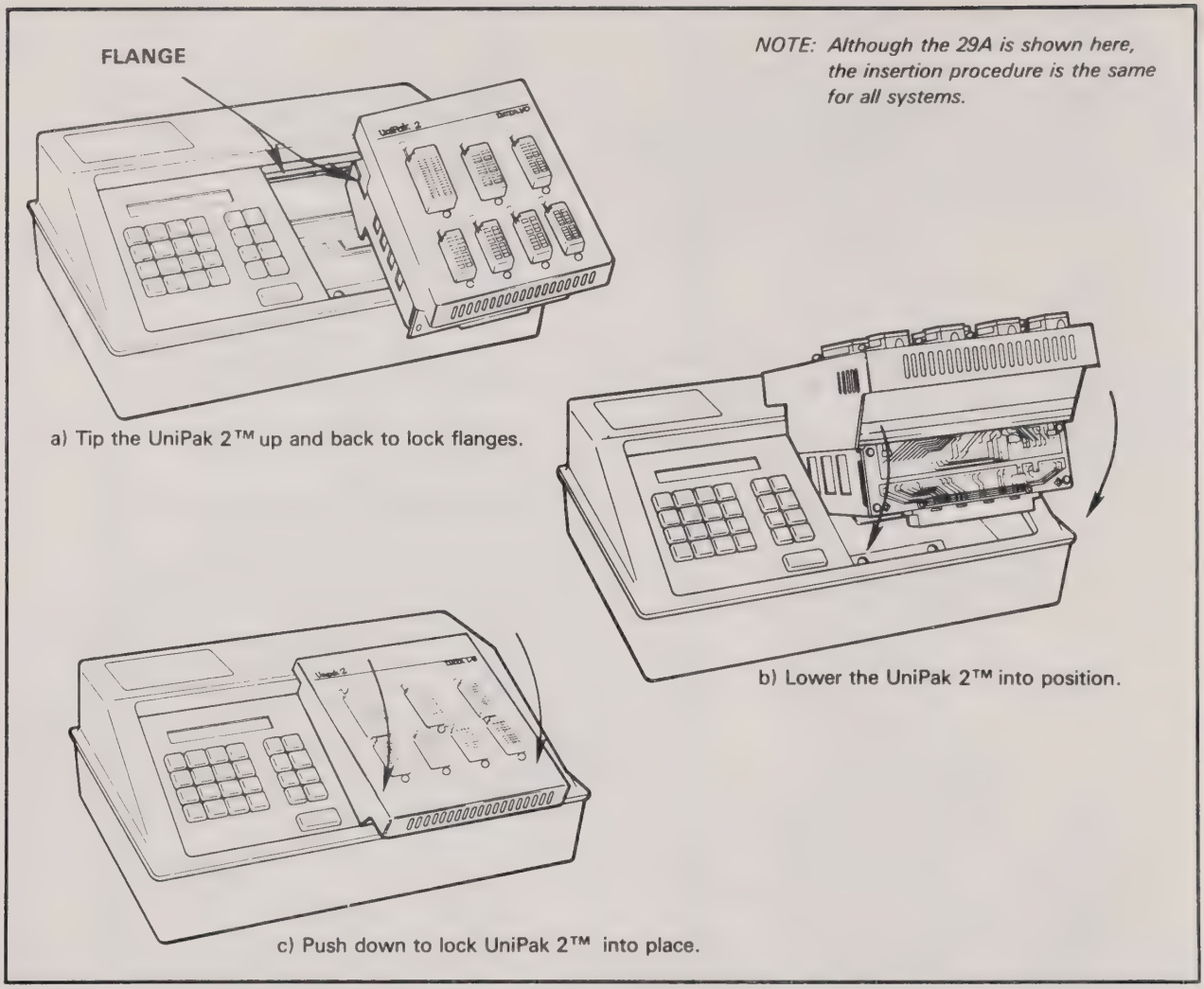

Figure 2-1. UniPak 2™ Installation

SECTION 3
OPERATION

3.1 OVERVIEW

The UniPak 2™ can be used in 29A, System 19 or 100A programmers of any configuration; see section 1.2 for firmware revision levels required. The typical programming operation with a 29A programmer and a UniPak 2™ is illustrated in figure 3-1. As can be seen from this figure, the UniPak 2™ can obtain data from three sources (a master device, a serial port, or from the keyboard); because the serial port and keyboard operation are unique for each type of programmer, you will be referred to your 29A, System 19, or 100A programmer manual for details on how to program using these mainframes.

When using a master device as the data source to program a blank device, you must first instruct the programmer to copy the device data into programmer RAM (shown as COPY on figure 3-1 and described in section 3.4), then enter the family code and pinout code as described in section 3.6. The data in the device will have been copied to the RAM of your 29A when you press START as shown in figure 3-1. You must then remove the master device and instruct the programmer to copy the information just stored in its RAM to a blank device. This completes the basic programming operation.

The procedures to perform basic operations with your UniPak 2™ are described in this section. These procedures have been provided in the order that they will have to be followed to operate your UniPak 2™. Wherever possible, key sequences have been included to use your UniPak 2™ with a 29A Universal Programmer with Rev C firmware (read section 1.2 carefully to determine your programmer's firmware revision level). Refer to your programmer manual for key sequences for the 19 and 100A programmers.

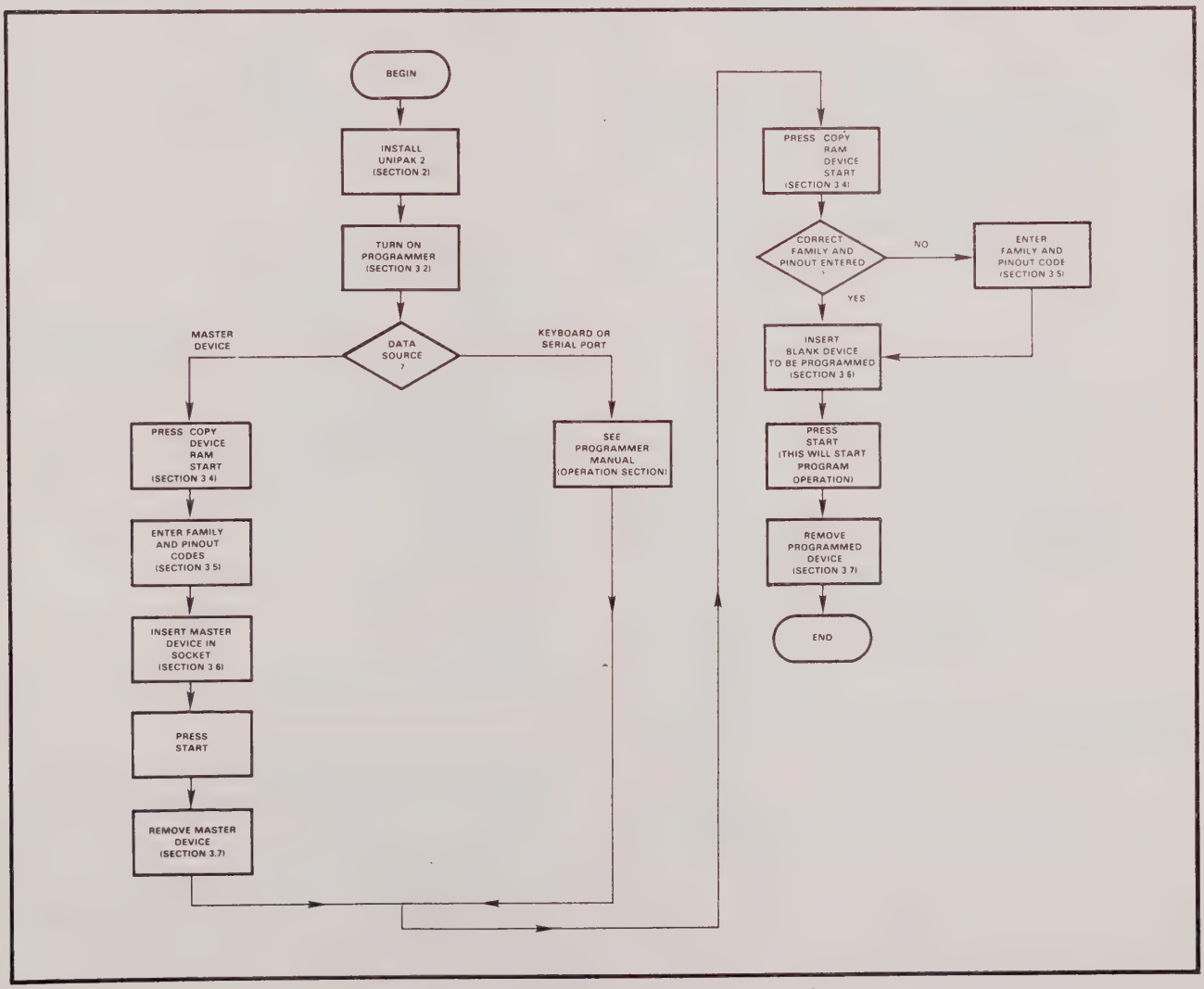

Figure 3-1. Typical 29A Programmer Operation

3.2 POWER UP

NOTE

If the UniPak 2™ is not installed in the programmer before power is turned on, you will hear a "beep" until the UniPak 2™ is installed.

When turned on, the programmer will perform an automatic self-test routine. When the self-test routine is complete, the programmer will signal its readiness.

To turn the programmer on, do the following.

1. Check to make sure a device is not in a socket. If a device is in a socket, lift up the lever (located on the upper left of the socket; see section 3.7) then gently lift the device out of the socket.

2. Plug the AC power cord into the power outlet.

3. Flip the power switch up to the "ON" position; see figure 3-2.

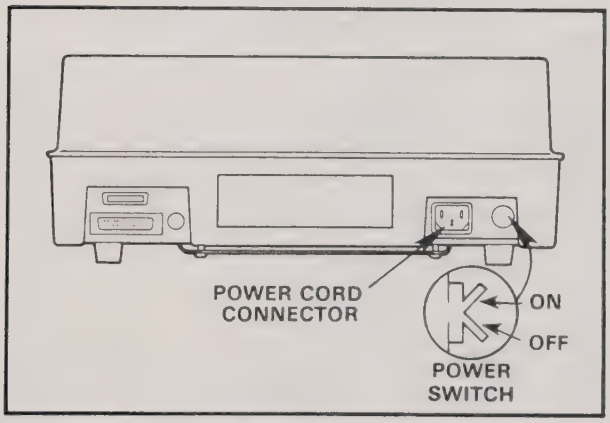

Figure 3-2. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.

To turn the programmer power off, do the following procedure:

1. Check to make sure that the programmer is not in the middle of an operation. If it is, wait until the operation is complete.

2. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.7.

3. Flip the power switch down to the "OFF" position (figure 3-2).

3.4 BASIC OPERATION

All data transfer or verification operations take place between the programmer's internal RAM and the device or between the RAM and serial port in your programmer. Because the operation procedure to transfer data via a serial port varies from programmer to programmer, this manual only describes data transfer with the 29A. For other programmers, refer to your programmer operation manual.

The basic data transfer operations that can be accomplished with the UniPak 2™ and 29A Universal Programmer are:

- load RAM with data from a master device (described in section 3.4.1),

- verify RAM data against the device data (described in section 3.4.2), and

- program a device with RAM data (described in section 3.4.3).

3.4.1 Load RAM with Data from Master Device

To load the 29A RAM with data from a master device, follow the steps listed below.

1. Press COPY; 29A displays COPY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE

The device is the source of data.

3. Press RAM; 29A displays CO DEV > RAM ∧ ADDR

NOTE

The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ∧ ØØ PIN ØØ.
5. Enter the family code and pinout code (see section 3.5).
6. Insert the master device into the UniPak 2™ (see section 3.6).
7. Press START; 29A displays LOADING DEVICE
   LOAD DONE XXXX

NOTE

XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak 2™ (see section 3.7).

During source destination operations (copy and verify) ADDR and SIZE appear in the 29A prompts. These correspond to starting address and block size, respectively. For more detail on these parameters, see your programmer operation manual. When reading a device, the UniPak 2™ applies a nominal V_{CC} level. To simulate loading on device outputs, each output is driven by a 1.6mA current source.

3.4.2 Verify RAM Data Against Master Device Data

The two-pass verify consists of comparing the device data to RAM data and is performed at two V_{CC} levels; these levels, plus the output-sink currents and the output-level-sense voltages, vary according to each manufacturer's requirements.

To verify that data entered in the 29A RAM duplicates the master device data, follow the steps listed below.

1. Press VERIFY; 29A displays VERIFY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE

The device is the source of data.

3. Press RAM; 29A displays VE DEV > RAM ∧ ADDR

NOTE

The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ØØ PIN ØØ.
5. Enter the family code and pinout code (see section 3.5).
6. Insert the master device into the UniPak 2™ (see section 3.6).
7. Press START; 29A displays VERIFY DEVICE
   VE DEV DONE XXXX

NOTE

XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak 2™ (see section 3-7).

3.4.3 Program Device with RAM Data

When programming a device, the system performs illegal bit tests and blank checks at nominal V_{CC} and with nominal output loading.

To program a blank device with the data in the 29A RAM, follow the steps listed below.

1. Press COPY; 29A displays COPY DATA FROM
2. Press RAM; 29A displays RAM ∧ ADDR/SIZE TO
3. Press DEVICE; 29A displays CO RAM > DEV ∧ ADDR
4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3-5).
6. Insert the blank device into the UniPak 2™ (see section 3-6).
7. Press START; 29A displays TEST DEVICE
   PROGRAM DEVICE
   VERIFY DEVICE
   PRG DONE 01 XXXX
8. Remove the device from the UniPak 2™ (see section 3.7).

NOTE

XXXX represents the sumcheck of the device.

3.4.4 Extended Select Functions

In addition to the three basic source-destination functions (copy, verify and edit) and the select functions described in the Operation Section of your programmer manual, the UniPak 2™ offers five extended select functions (CC, CD, CE, CF and EF). These functions are not required for normal operation of the UniPak 2™.

Functions CC and CD are used in conjunction with electronic identifiers and may be used from the keyboard or from remote control.

Function CC displays the family and pinout codes of the last algorithm moved to RAM, usually the algorithm for the last device programmed or read. This function helps determine the family and pinout codes used by the programmer when in the automatic electronic identifier mode.

Function CD displays in hexidecimal 16 bytes of the device's electronic identifier. Byte Ø identifies the manufacturer; byte 1 identifies the device. For information on the purpose of the remaining bytes, consult the device data sheets.

To display the family and pinout codes of the last algorithm moved to RAM, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CC START; 29A displays XXYY **

NOTE

XX represents the family code; YY represents the pinout code.

To display the electronic identifier follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CD START; 29 A displays 0000 YY
3. To display additional bytes of electronic identifier press START; 29A displays 000X YY. To back up through previously displayed identifiers press REVIEW; 29A displays 000X YY

NOTE

000X represents the byte number of the identifier displayed (i.e., 0001 represents byte 1 of the electronic identifier which is the device code). YY represents the identifier byte in hexidecimal.

Functions CE and CF are used to set the reject count (the number of programming pulses applied to a fuse or cell before it is rejected); CE sets the reject count back to the commercial specification (this is the default value) and CF sets the single pulse reject count. This feature was accomplished in older UniPak models by adding 50 to the family code).

To select the commercial (default) reject count (CE) follow the procedures below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CE START; 29A displays SELECT CODE **

To select the single pulse reject count (CF) follow the procedures below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CF START; 29A displays SELECT CODE **

Function EF calls up a 4-digit hexadecimal configuration number that corresponds to the revision level of the UniPak 2™ firmware. This function can be useful to identify firmware revision levels when communicating with Data I/O regarding Field Bulletins and updates.

To display the UniPak 2™ firmware configuration number, do the following.

1. Press SELECT; 29A displays SELECT CODE ∧

2. Press EF START; 29A displays XXXX **

NOTE

XXXX represents the UniPak 2™ firmware configuration number.

3.5 ELECTRONIC IDENTIFIERS

This version of UniPak 2™ can read and use electronic identifiers in two modes.

The first mode occurs when family code 79 or 93 is selected. The identifier is read and used to prohibit programming a device using the wrong family and pinout codes. The new low Vpp devices are protected from the old high Vpp algorithms which might destroy them. Older devices without signatures are permitted to program. An error will occur if programming is attempted using the wrong family or pinout codes.

The second mode is automatic. It is selected by entering family and pinout codes FF/FF. In this mode the operator need not look up any family or pinout codes; the electronic identifier is read and the correct algorithm is used for each device. An error will occur if programming is attempted on older devices without electronic identifiers or on newer devices whose identifiers are not yet supported.

3.6 FAMILY CODE AND PINOUT CODE SELECTION

Any device that can be programmed with the UniPak 2™ is specified by a unique combination of 2-digit family code and a 2-digit pinout code (table 1-2). Once the codes are entered for a particular device, the UniPak 2™ remains set up for any operation with that device until new codes are entered.

Your programmer manual will tell you where in the key sequence the family and pinout codes should be entered. If invalid family and pinout codes are entered, a beep will sound as either START or ENTER is pressed, or error 30 will be displayed and the operation will be aborted.

To select the family and pinout codes, do the following procedure.

1. Locate the manufacturer and part number stamped on the device.

2. Go to table 1-2, column 1 and find the manufacturer's name.

3. Go to table 1-2, column 3 entitled "PROM Part Number" and find the number corresponding to the number on the device.

4. Go to column 4 ("Family Code") and column 5 ("Pinout Code") to find the code numbers corresponding to the device number.

5. Enter the family code and pinout code you selected from table 1-2.

6. Push "START".

NOTE

An LED (light emitting diode) will light up under one of the sockets.

Valid family and pinout codes must be in effect to use the System 19 DEVICE DATA key. When the DEVICE DATA key is pressed, either nominal, first-pass, or second-pass verify levels are applied to the device. The level applied depends on the 19's position in executing the selected mode. If the KEYBD light is on, the nominal verify level is applied.

3.7 DEVICE INSERTION

Once you have chosen the appropriate family and pinout codes, the UniPak 2™ is ready to accept a device in the socket located above the lighted LED.

NOTE

In the automatic electronic identifier mode no LED is lighted unless UniPak 2™ is performing an operation on a device. An empty socket will always be unlighted. In this mode, disregard any reference to lighted LEDs; use the socket with the correct number of pins.

A good electrical connection between the device and the socket is essential. To ensure a good connection, do the following.

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.

2. Lift up the lever on the upper left side of the socket above the lighted LED; see figure 3-3. (The lever will stay locked into the upright position.)

3. Gently set the device in the socket above the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket as shown in figure 3-3.

4. Push the lever down to lock the device in the socket.

Once the family and pinout codes have been entered, the UniPak 2™ is ready for device-related operations. The key sequence to load, program, and verify are described in the operation section of your programmer manual.

3.8 DEVICE REMOVAL

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.

2. Lift up the lever on the left side of the socket; see figure 3-3. (The lever will lock into the upright position.

3. Lift the device out of the socket; the LED will remain illuminated.

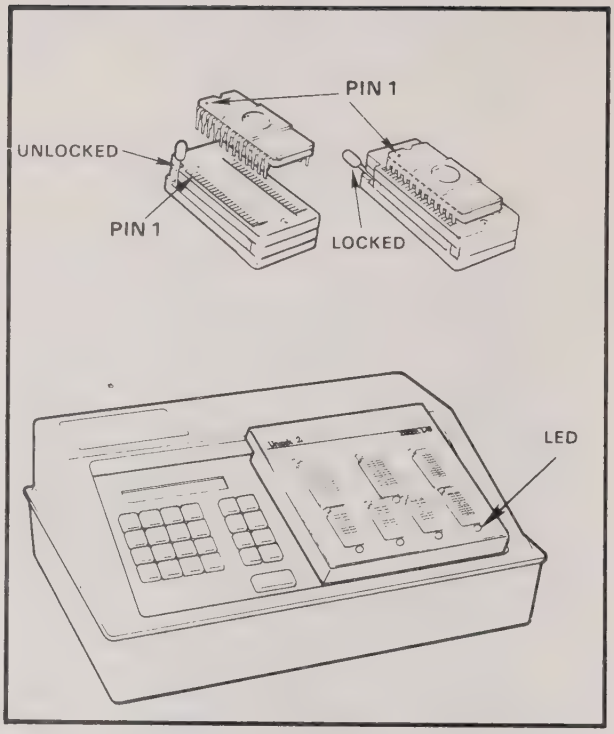

Figure 3-3. UniPak 2™ Sockets and Device Installation

SECTION 4
MAINTENANCE/TROUBLESHOOTING/ CALIBRATION

4.1 OVERVIEW

The support material in this section has been provided to help you keep your UniPak 2™ in good operating condition. General maintenance practices are discussed in section 4.2 while the basic troubleshooting steps are listed in section 4.3. For those UniPak 2™ users who prefer to do their own calibration, detailed procedures including measurement charts and timing diagrams are provided in section 4.4.

4.2 MAINTENANCE

Before the UniPak 2™ can be cleaned (section 4.2.2) and/or inspected (section 4.2.3), it must be disassembled as described below.

4.2.1 UniPak 2™ Disassembly

To disassemble the UniPak 2™, refer to figure 4-1 and the procedures listed below.

1. Remove the UniPak 2™ from the programmer; see section 2.3 for details.
2. Lay the UniPak 2™ face down on a flat surface.
3. Unscrew the captive fasteners (figure 4-1a) until they hang loosely; the screws will not separate from their stand offs.
4. Lift the card cage up slightly, then pull out (as shown in figure 4-1b) to unlock the flanges.
5. Lift the card cage up until you can see the socket board interconnect cable and its connector (figure 4-2).
6. Flip the extraction tabs out on each side of the connector (figure 4-2).
7. Pull the cable out of the connector.
8. Disconnect the ground wire from the socket board (see figure 4-2).
9. Flip the extraction tabs out on the top card (waveform generator card) and unplug the interconnect cable from its connector (figure 4-3).
10. Flip the extraction tabs out on the top card (waveform generator card).
11. Pull the waveform generator card out along the guides (figure 4-3).
12. Repeat steps 9, 10, and 11 for the extraction tabs on the address card.

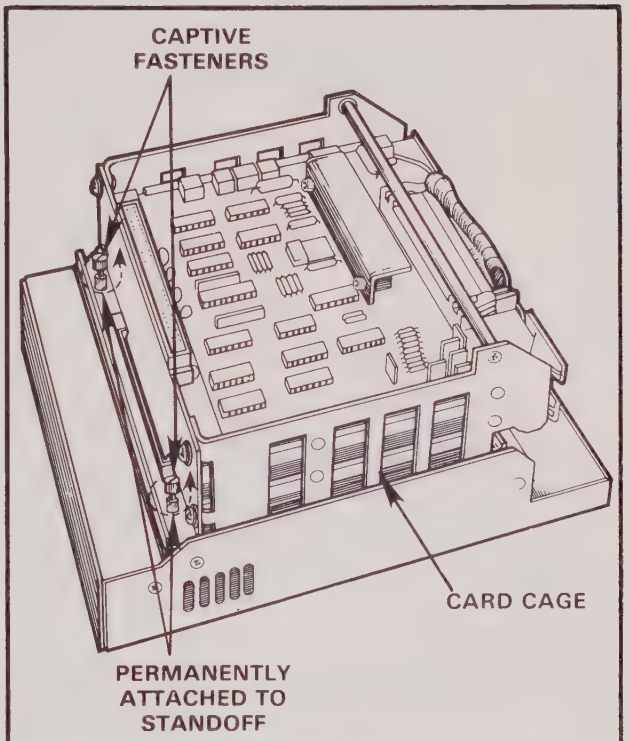

Figure 4-1a) Unscrew Captive Fasteners

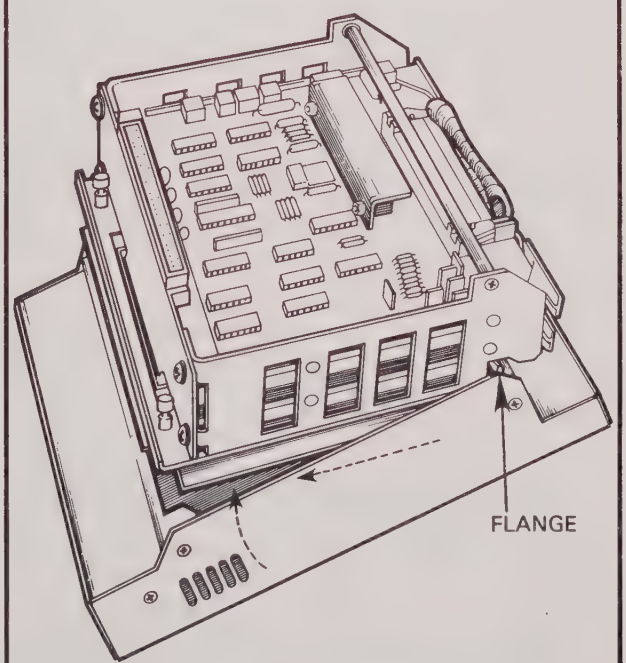

Figure 4-1b) Lift card cage up and out.

Figure 4-1. UniPak 2™ Disassembly

13. Remove the two screws and shield, and pull the memory card down to unplug it from the edge connector (as shown in figure 4-4).

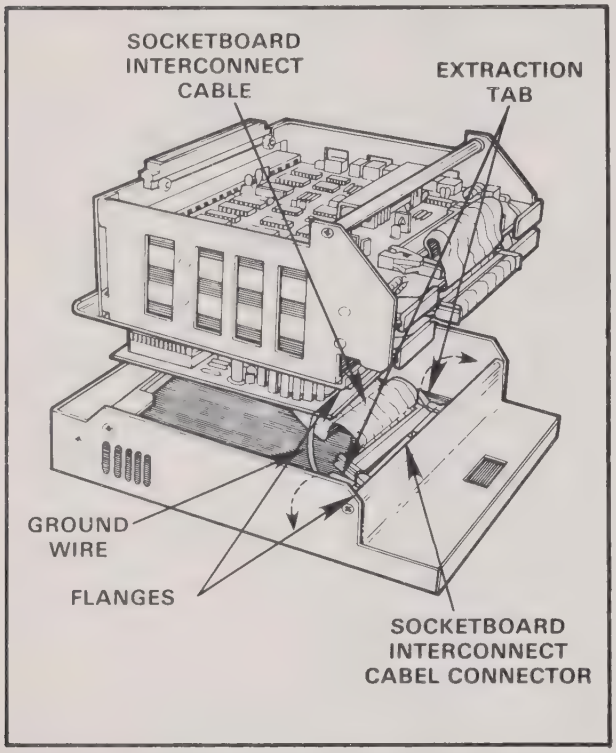

Figure 4-2. Socketboard Interconnect Cable Disconnect

4.2.2 Cleaning

Inspect the UniPak 2™ inside and out for accumulated dirt or dust. To clean the UniPak 2™, follow the procedures below.

1. Wipe any dust and/or dirt off the outside of the UniPak 2™ with a clean, damp cloth.

NOTE

Do not use abrasive cleaners or solvents which will etch the paint.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

4.2.3 Inspection

You can help prevent malfunctions by periodically inspecting your UniPak 2™. Check cable connections, card seating, mounting of socketed components, etc. for shorts, opens or unstable continuity.

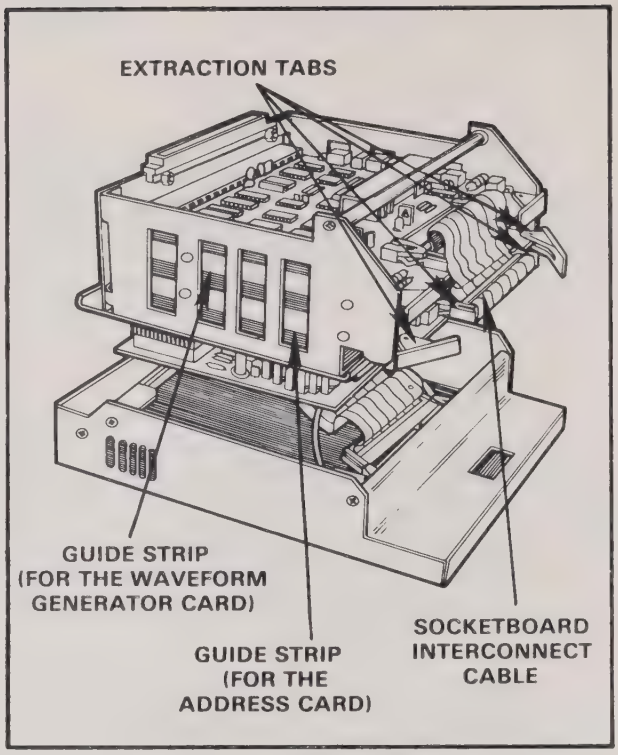

Figure 4-3. Circuit Board Removal

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This will prevent further damage.

4.2.4 UniPak 2™ Assembly

1. Plug the memory card onto its edge connector as shown in figure 4-4.

2. Replace the shield, washers, and two screws.

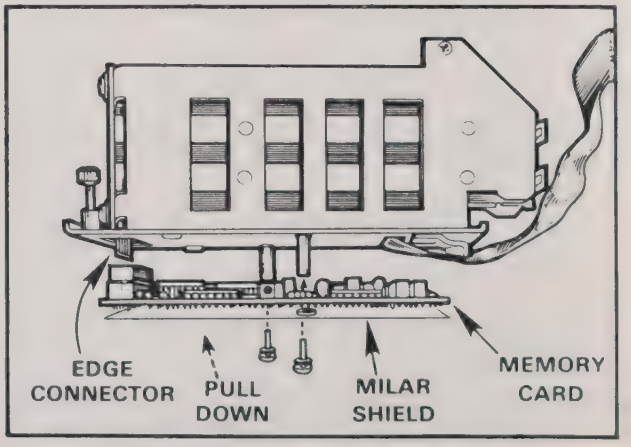

Figure 4-4. Memory Card Removal

3. Flip the two extraction tabs down on the address card.

4. Using the flat surfaces of the extraction tabs, gently push the address card along the guides into its connector.

5. Make sure the extraction tabs on the interconnect cable connector are flipped open.

6. Firmly, but gently, push the socket board interconnect cable into the connector. Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.

7. Repeat steps 3-6 to replace the waveform generator card.

8. Reconnect the ground wire to the socket board.

9. Plug the socket board interconnect cable into its connector on the socket board (figure 4-2).

10. Replace the card cage by tilting it up to lock the flanges as shown in figure 4-1, then gently setting it down. Make sure the captive fasteners line up with the fastener holes on the UniPak 2™ frame.

11. Tighten the captive fasteners finger tight.

4.3 TROUBLESHOOTING

This section is intended to help you interpret and isolate failures in the UniPak 2™. It should be used in conjunction with section 5 (Circuit Description) and the schematics provided in the back of this manual.

There are three major classes of failures that can occur in a system comprised of a programmer and a UniPak 2™. The first is no system operation, the second is poor yields, and the third is UniPak 2™ failure.

After successfully troubleshooting the UniPak 2™, it must be calibrated according to the instructions in section 4.4. It is very important that the programmer be calibrated before the UniPak 2™ is calibrated.

4.3.1 No System Operation

The following steps should be performed if the system will not initialize with the UniPak 2™ installed. After completing each step, determine whether the problem still exists.

1. Check to be sure the UniPak 2™ is properly installed in your programmer.

2. Check the UniPak 2™ programmer mating connector (J1) for bent or broken pins. (Pin HH is intentionally shorter.)

3. Check the UniPak 2™ cards to be sure they are correctly installed in their connectors (section 4.2).

4. Check the ribbon cable to be sure it is properly inserted in the connectors (section 4.2).

5. Check the programmer power supplies for proper voltage output levels (see programmer manual).

6. If steps 1 through 5 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.2 Poor Yields

The following steps should be performed if the yield rate begins to decrease. After completing each step, determine whether the problem still exists.

1. Perform a complete calibration; be sure that the programmer has been calibrated first.

2. Perform waveform observations (section 4.4) for the family of the device being programmed, being careful to note any discrepancies. The Circuit Description (section 5) and the schematics at the end of this manual may be useful in isolating the problem.

3. Perform calibration steps 27 and 28 on the measurement chart for the device family that is giving problems. The Circuit Description (section 5), schematics, and suspected components in tests 1 through 4 of Table 4-1 may be helpful in isolating the problem.

4. If steps 1 through 3 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.3 UniPak 2™ Failure

The following steps should be performed if a device will not program at all or if error messages are displayed. After completing each step, determine whether the problem still exists.

1. Check that the family and pinout codes are correct for the device, and that the device is being inserted in the correct socket.

2. If possible, try a known good device to determine if it is a hardware problem.

3. Check to be sure the UniPak 2™ is properly installed.

4. Check the UniPak 2™ programmer mating (J1) connector for bent or broken pins. (Pin HH is intentionally shorter.)

5. Check the UniPak 2™ cards to be sure they are correctly installed in their connectors (section 4.2).

6. Check to be sure the ribbon cable is correctly oriented and properly inserted in the connectors.

7. Perform a complete calibration noting any measurements falling outside of the indicated limits. Refer to the corresponding test number in table 4-1 for suspected boards and components, as well as the Circuit Description (section 5) and the schematics to attempt to isolate the problem.

8. Perform waveform observations and note any discrepancies. Referring to the Circuit Description and the schematics may be helpful in isolating the problem.

9. If steps 1 through 8 fail to isolate the problem, contact your local Data I/O Service Center.

Table 4-1. Troubleshooting Chart

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
1	701-1655	VR1, U17, U25
2	701-1655	VR1, U16, U25, Q2, Q3
3	701-1655	VR1, U16, U25, Q2
4	701-1690 702-1659	U15, U7, U12, Q21, R52, CR15, CR16, VR1, Q15 CR18, U10
5	701-1690 702-1659	U14, U7, U3, Q3, R15, CR4, CR3, U10, U9, U11, Q24, Q25, Q19, CR14, Q16, U18, U17, VR1, Q15 C5, R11, CR9
6	701-1690 701-1655	U13, U7, U6, Q9, R31, CR10, CR11, Q2, CR19, VR1, Q15 U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, U24, U11, CR6
7	702-1650 702-1659 701-1655	U23, U22, VR2, CR3, Q2, R28 CR24, Q10, U20 U4, U14
8	701-1655	VR1, U17, U25
9	701-1655	VR1, U16, U25, Q2
10	701-1655	VR1, U17, U25
11	702-1650 701-1655	U17, Q3, R3, VR1, U2, Q1, CR1, CR2 U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, CR6, U24, U11
12	702-1650 701-1655	U17, Q3, R3, VR1, U2, Q1, CR1, CR2, VR3, U5, U22, U11 U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, U24, U11, CR6
13	701-1690 701-1655	U17, U18, U11, Q22, Q25, Q2, CR19 U23, R1, RP8, Q16, RP3, Q14, RP4, RP2, Q12, U19, U24, CR9
14	701-1690 702-1659	U15, U7, U12, Q21, U16 CR18, U10
15	701-1690	U16, U13, U7, U6, Q9
16	701-1690	U16, U14, U7, U3, Q3
17	701-1655	U26, U17, U25, VR1
18	701-1655	U26, U16, U25, VR1, Q2
19	702-1650 701-1655	U5, U22, U17, U11, Q3, U2, CR1, CR2, Q1 U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR6, U11, U24
20	701-1690, 701-1655, 702-1659	
21	702-1659 701-1655	U4, DS2 U18
22	701-1690 702-1659	U15, U7, U12, Q21, CR15, CR14, U16 CR18, U10

Table 4-1. Troubleshooting Chart (continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
23	702-1659	CR26, Q6, Q7, Q5
	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1650	U16, U3, U10, U12, U11, U7
24	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, Q19, CR14, Q16, CR4, CR3
	702-1659	C5, R11
25	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8, CR4, CR3
	702-1659	C5, R11
26	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q4, Q10, Q12, Q5, Q7, CR4, CR3
	702-1659	C5, R11
27	701-1690	U16, U13, U7, U6, Q9, CR10, CR11, Q2, CR19
	701-1655	U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9, U19, U24
28	701-1690	U16, U13, U7, U6, Q9, Q2, Q18, U17, Q11, CR2, Q14, U5
29	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
30	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8
	702-1659	C5, R11
31	702-1650	U23, U22, VR2, CR3, Q2, R28
	702-1659	CR24, Q10, U20
	701-1655	U4, U14
32	701-1690	U18, U10, U5, U7, Q20, Q7, Q5, Q12, U9, CR9, Q13, U11, Q24
	702-1659	CR8, C5, R11
33	701-1690	U11, CR17, VR2, U18, Q19, Q16, U9, Q24, U10
	702-1659	CR9, R11, C5
34	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1659	CR4, CR3, CR2, U22, CR5, Q1, CR32, CR31, CR28, C3, C13
	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
35	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
36	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
37	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q7, Q5, Q12, Q20, U7
	702-1659	C5, R11
38	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1659	CR4, CR3, CR2, U22, CR5, Q1, CR32, CR31, CR28, C3, C13
	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U24, U11, U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR9
39	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
40	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7
	702-1659	Q2, CR29, R30, CR28, CR31, CR32

Table 4-1. Troubleshooting Chart (continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
41	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19, CR4
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
42	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19, CR4
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
43	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
44	702-1659	DS1, U4
	701-1655	U18
45	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR7, U10
46	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
47	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
48	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
49	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
50	701-1655	Q4, Q8, Q12, Q5, Q14-17, U23
51	701-1655	Q6, Q11, Q9, Q7, Q14-Q17, U23
52	701-1655	Q4, Q8, Q12, Q5, Q14-17, U23
53	701-1655	Q6, Q11, Q9, Q7, Q14-17, U23
54	702-1659	DS3, U4
	701-1655	U18
55	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR22, U10
56	702-1659	DS4, U4
	701-1655	U18
57	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR1
58	702-1659	DS5, U4
	701-1655	U18
59	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR11
60	702-1659	DS6, U4
	701-1655	U18
61	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR19
62	702-1659	DS7, U4
	701-1655	U18

Table 4-1. Troubleshooting Chart (continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
63	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR23
64	702-1659	Q3, CR14, RP1, R10, CR17, U10
	701-1655	U18, U22
65	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1
	702-1659	CR17, CR1, CR11, CR19, CR23, CR22, CR7, CR18, U10
66	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1
	702-1659	CR17, CR1, CR11, CR19, CR23, CR22, CR7, CR18, U10

4.4 CALIBRATION

The need for calibration varies with the amount of use your UniPak 2™ receives. Generally, we suggest calibration whenever: 1) programming yields fall below the manufacturer's recommended minimums; or 2) when troubleshooting has been completed; or 3) if the user's company policy requires periodic calibration certification.

NOTE

If calibration or repair is required but you lack the facilities to accomplish it, contact the nearest Data I/O service center.

Because of the different programmer mainframes, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the UniPak 2™.

Calibration of the UniPak 2™ consists of three parts:

1. Power Supply Calibration—measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.

2. DC Calibration—consists of measuring and adjusting critical DC voltage levels generated by the UniPak 2™.

3. Waveform Observation—enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

The first part of the calibration procedure (power supply calibration) varies with the type of programmer you have. Therefore, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in section 4.4.1 the optional verify voltage checks are described in 4.4.2, and waveform observation is detailed in section 4.4.3. For information on how to carry out these steps on various programmers, consult your programmer manual.

The following equipment is necessary to calibrate the UniPak 2™:

- Data I/O Calibration Extender (part number 910-1521)
- Three and a half digit digital voltmeter (DVM)
- Dual-trace Oscilloscope (Tektronix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that you may need to calibrate the programmer.

To prepare your UniPak 2™ for calibration, follow the procedures listed below.

1. Turn the programmer power off; see section 3.3 for details.

2. Remove the UniPak 2™ from the programmer; see section 2.3 for details.

3. Insert the calibration extender into the programmer the same way you insert the UniPak 2™ (section 2.2).

4. Unscrew the two thumb screws (captive fasteners) located on the underside of the top cover of the UniPak 2™ (figure 4-1); they connect the card cage to the socket assembly. Separate the two parts of the assembly.

CAUTION

Do not let the fasteners short to the motherboard.

5. Insert the 64-pin connector of the card cage into the mating connector on the calibration extender (figure 4-5b).

6. Lean the top portion of the UniPak 2™ against its bottom portion at a 45-degree angle; see figure 4-5.

NOTE

Be sure the socket assembly flange locks into the card cage flange (see figure 4-5b).

Do not allow the frame of the socket assembly to short to the memory board.

Be careful not to strain the cable or scratch the top of the programmer.

4.4.1 DC Calibration

The DC calibration procedures described in this section enable you to adjust critical DC voltage levels generated by the UniPak 2™. To follow these procedures, use the measurement chart at the end of this section. This measurement chart contains the information necessary for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.—tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.—identifies individual tests.
- Test Description—identifies the functions being tested.
- Measurement Test Location—tells which socket pins, circuit boards, or test points to probe for measuring voltages.

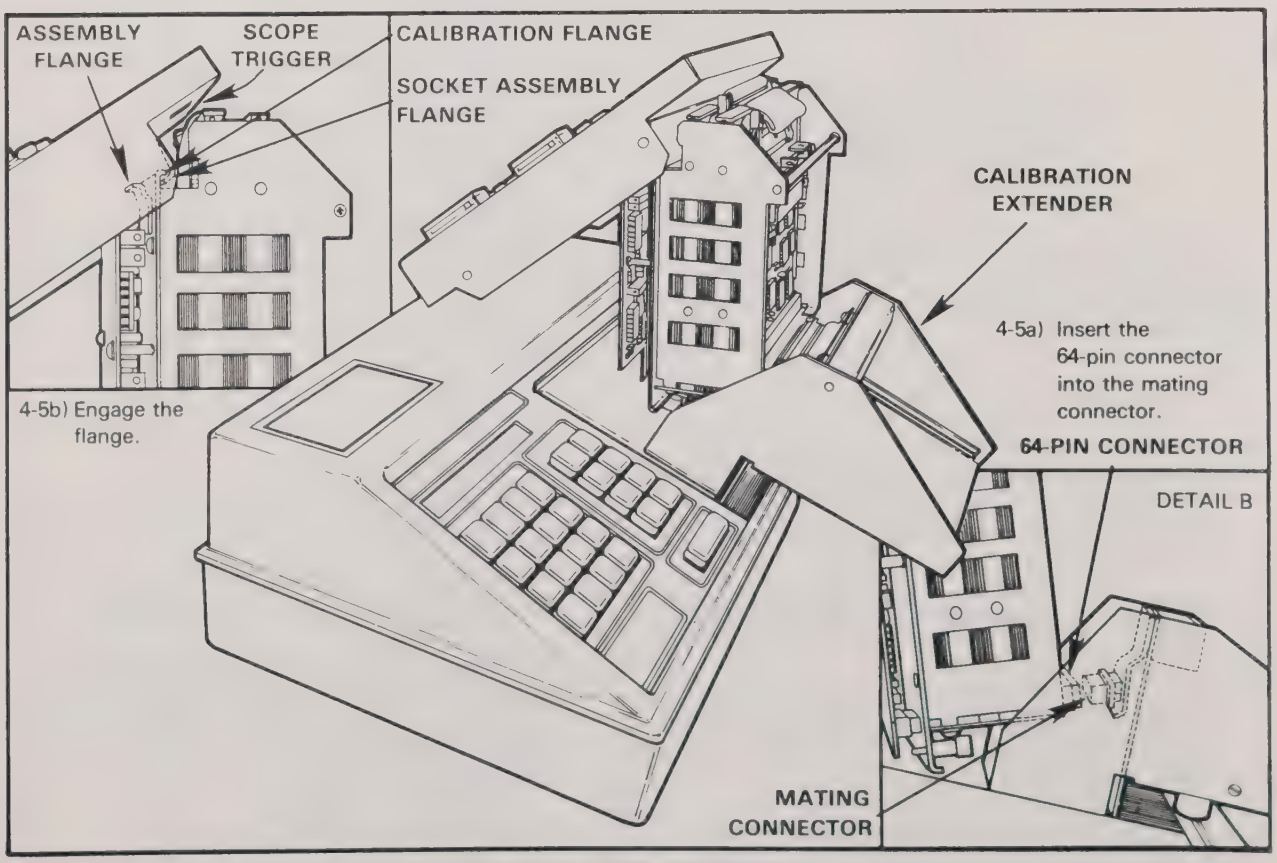

Figure 4-5. Calibration Set-up

- Measurement—specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the UniPak 2™ until the problem is corrected.
- Adjustment Location—tells which potentiometer to adjust if a measurement is out of range.
- Comments—gives special instructions for particular tests.

The DC calibration procedures are as follows:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.8 for details). Waveform generation may damage any device in the UniPak 2™ sockets.

1. Turn the programmer power on (section 3.2).
2. Put the programmer into the calibration mode by following the key sequences in table 4-2.
3. Perform the general calibration steps (steps 1-24) on the measurement chart. For steps 5, 6 and 7, refer to the figures at the end of the measurement chart to observe the bit switch rise waveform, the DAC step waveforms, and the current DAC step waveform.

For each general calibration step on the measurement chart do the following:

- Take measurement readings at the device sockets or test points indicated in the measurement chart; figure 4-6 shows the pin numbers for the sockets; figure 4-7 shows test points.
- Ground the digital voltmeter to socket 7, pin 10 on the front panel of UniPak 2™.
- The adjustment pots on the waveform generator, the memory board, and the address card enable you to make adjustments when your measurements do not match the measurement chart; figure 4-7 shows the location of these adjustment points.
- Access each new step by pressing the START (or ENTER) key. The new step number will appear on the display when the UniPak 2™ is ready for the next step. To go back to a previous test, press the REVIEW (or BACKSPACE) key.

Table 4-2. Key Sequence to Access the Calibration Mode

Programmer System	Key Sequence to Enter Calibration Mode	Increment Step No.	Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number (a) Press START	Enter	Review
29A	Press SELECT Press C1 Press START Enter Step Number (a) Press START	Start	Review
100A	Press SELECT Press 12 Enter Step Number (a) Press START	Start	Back-space

(a) Optional

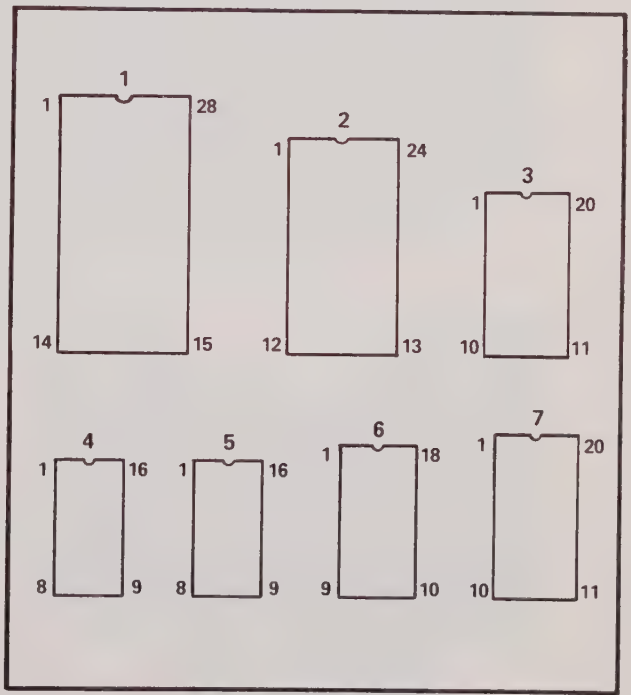

Figure 4-6. Pin Numbers of Device Sockets

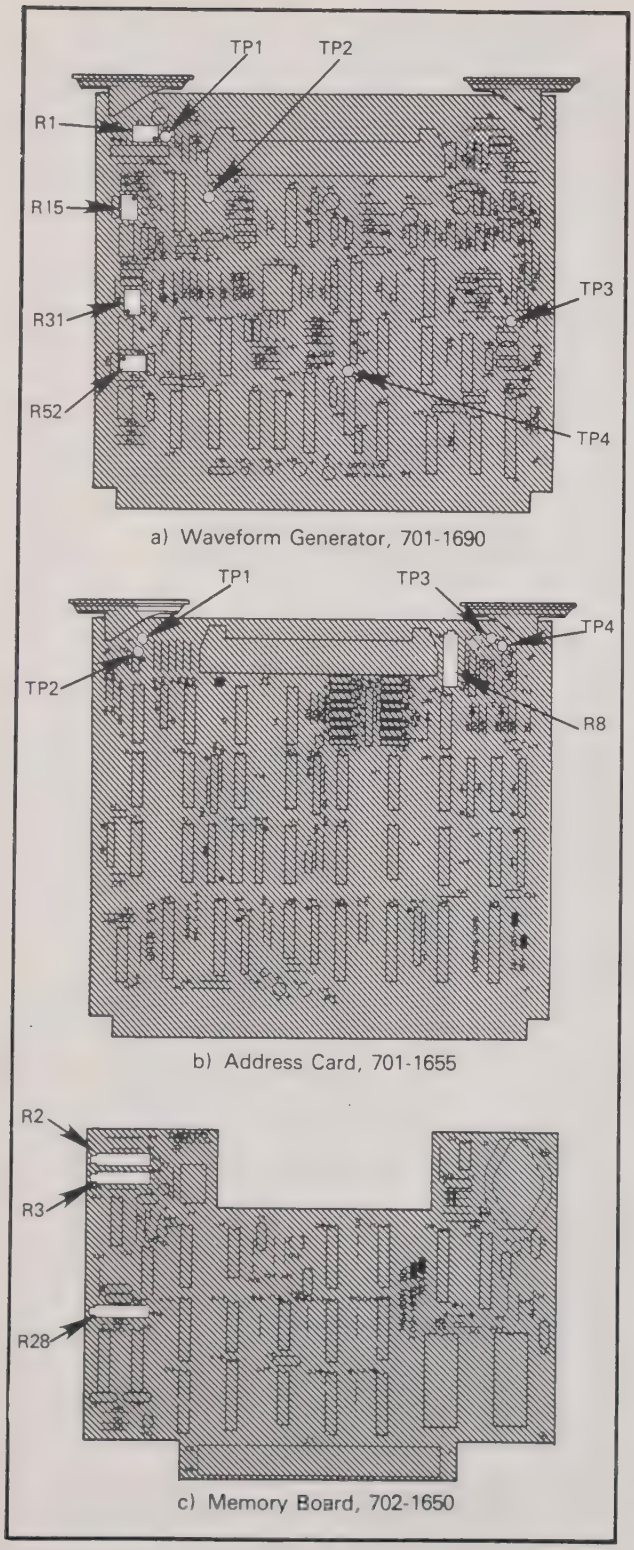

Figure 4-7. Adjustment Locations

NOTE

The remaining steps on the measurement chart (steps 25-28) are family-specific. These steps are optional and have been included for your convenience.

4. For each family-specific calibration step on the measurement chart, do the following to enter the family pinout codes.

   - Perform a **load operation**; refer to your programmer manual for details.
   - Enter the family and pinout code when prompted by the programmer; refer to your programmer manual for further information.
   - Fill RAM with data specified on the timing diagram.
   - Put the programmer back into the calibration mode; see figures 4-8, 4-9 and 4-10 for the key sequence.
   - Enter the step number from the measurement chart.
   - Press START.

4.4.2 Optional Verify-Voltage Checks

Two calibration steps (27 and 28) have been provided for the measurement of first and second pass verify voltages. The family characteristics table in the applicable family timing diagram defines the levels for first and second pass verifications for each family. These are provided for the investigation of yield problems; no adjustments are available. Under normal circumstances, these steps can be eliminated from a routine calibration.

4.4.3 Waveform Observation

Programming waveforms of your UniPak 2™ can be observed with an oscilloscope and compared with the timing diagrams that have been provided at the end of this section. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the UniPak 2™ is performing to the device manufacturer's specifications. Since the UniPak 2™ generates a large number of waveforms and all calibration adjustments are accomplished in DC calibration, it is only necessary to observe waveforms for commonly used devices or those that are presenting yield problems.

During the waveform observation phase of the calibration procedure, your UniPak 2™ uses a firmware routine that generates programming waveforms for the data stored in system RAM. An oscilloscope trigger pulse is generated for every address increment. This occurs after the reject pulse count has been reached for all the bits being programmed in the previous data word. The address is automatically reset to Ø when the maximum PROM address is reached, and incrementing

continues. Waveform observation can be done with the UniPak 2™ either on the calibration extender or plugged into the programmer.

The waveform observation procedure described below calls for filling RAM with data so that it is possible to observe bit-to-program waveforms. The procedure takes into account the device type (VOL of VOH) so that for either type of PROM a bit-to-program will appear on the same socket contact.

When used with a timing diagram, this procedure allows you to compare waveforms on the oscilloscope with the waveform photographs on the timing diagram for any type of device; a detailed explanation of the timing diagrams is provided in section 4.4.4. The waveform observation procedure is as follows:

1. Refer to table 1-2 to determine the family and pinout codes, polarity, and technology of the selected device.

NOTE

Polarity is indicated in the Family code. Odd numbered families are VOL and even numbered families are VOH.

2. Initiate a load operation; refer to section 3.4 for details.

3. Key in the family and pinout codes when prompted by the programmer; see section 3.5.

4. Fill your programmer's RAM with programming data listed in the timing diagram for the family code entered: the correct data depends on the polarity and technology of the device. Refer to table 4-3 for the "Fill RAM" key sequence.

CAUTION

Remove all devices before entering the calibration mode. Waveform generation may damage any device in the UniPak 2™ sockets.

5. Enter the waveform generation mode at step 27 on the measurement chart by following the key sequences listed in table 4-3.

6. Erase waveforms for EEPROMs are observable at step 28 of the measurement chart by following the key sequences listed in figure 4-8, 4-9 or 4-10 depending on your programmer.

7. Trigger your oscilloscope by connecting to the test point under the top edge of the socket assembly (see figure 4-11).

Table 4-3. Key Sequence to Fill RAM With Data

System	Key Sequence
19	Press SELECT A 2 Press ENTER Enter data Press START
29A	Press SELECT A 2 Press START Enter data Press START
100A	Press SELECT 1 3 Enter Password (SHIFT 2/ BACKSPACE) Enter data Press START

8. Ground the scope to the GND contact of the socket with its LED illuminated; the GND contacts are shown on figure 4-12.

9. To observe individual waveforms, refer to figure 4-13 under the pinout code number entered in step 3. The individual socket illustrations give the numbers of the socket contacts to probe when observing the waveforms on the timing diagram.

NOTE

Considerations helpful in setting up and interpreting the waveform displays are explained in section 4.4.4.

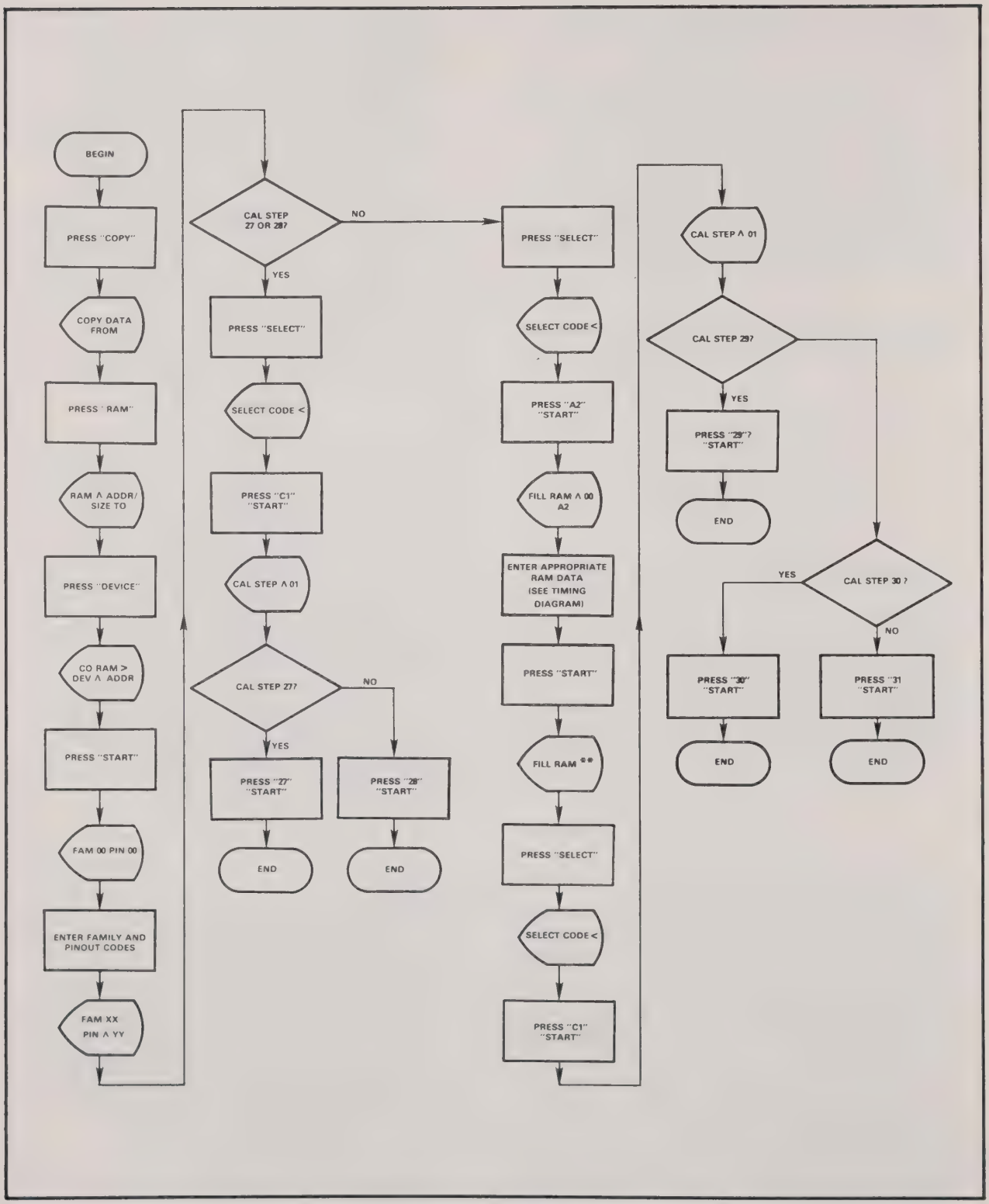

Figure 4-8. Accessing Calibration Steps 27, 28, 29, 30, 31 (29A Universal Programmer)

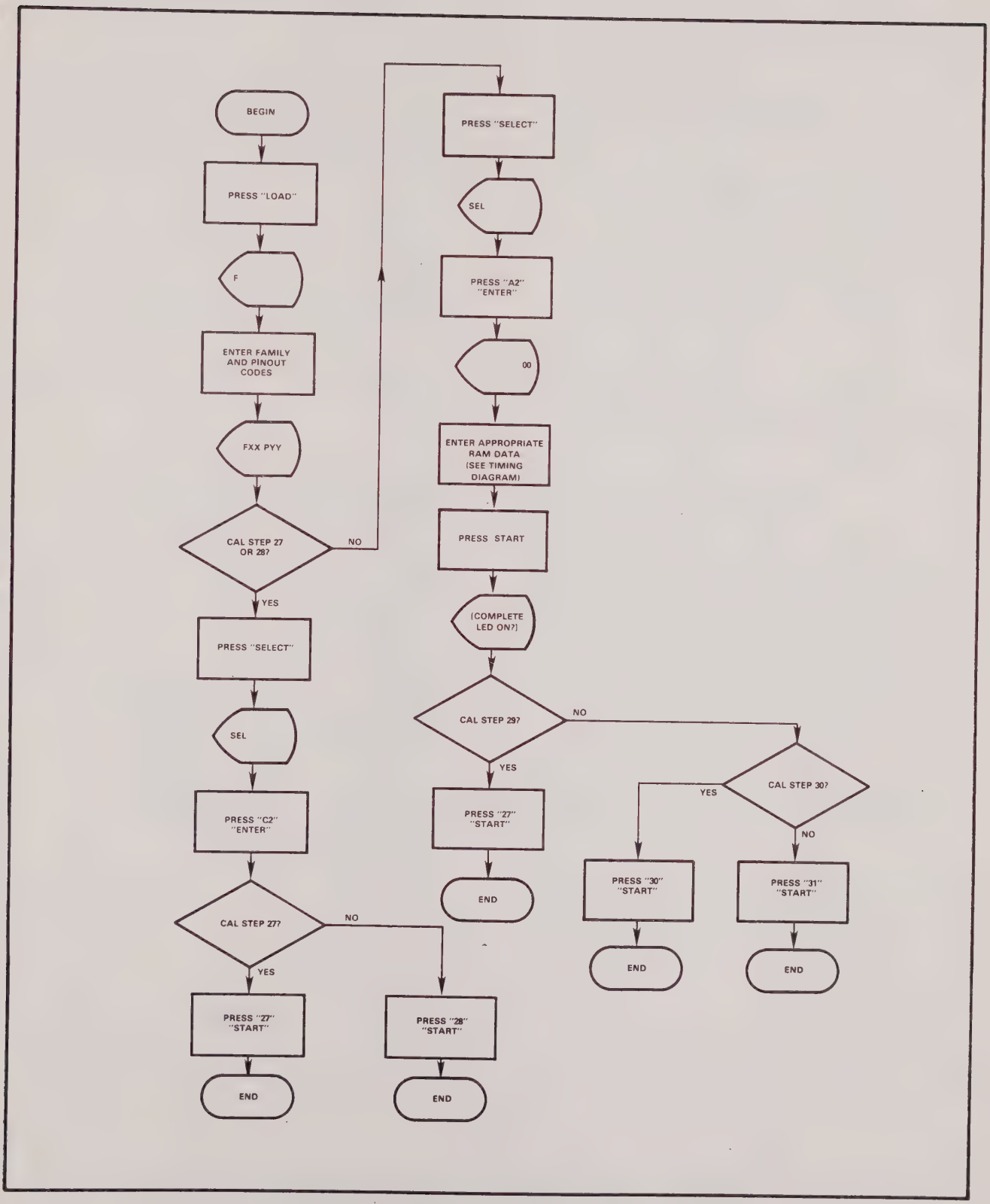

Figure 4-9. Accessing Calibration Steps 25, 26, 27, 28 (System 19)

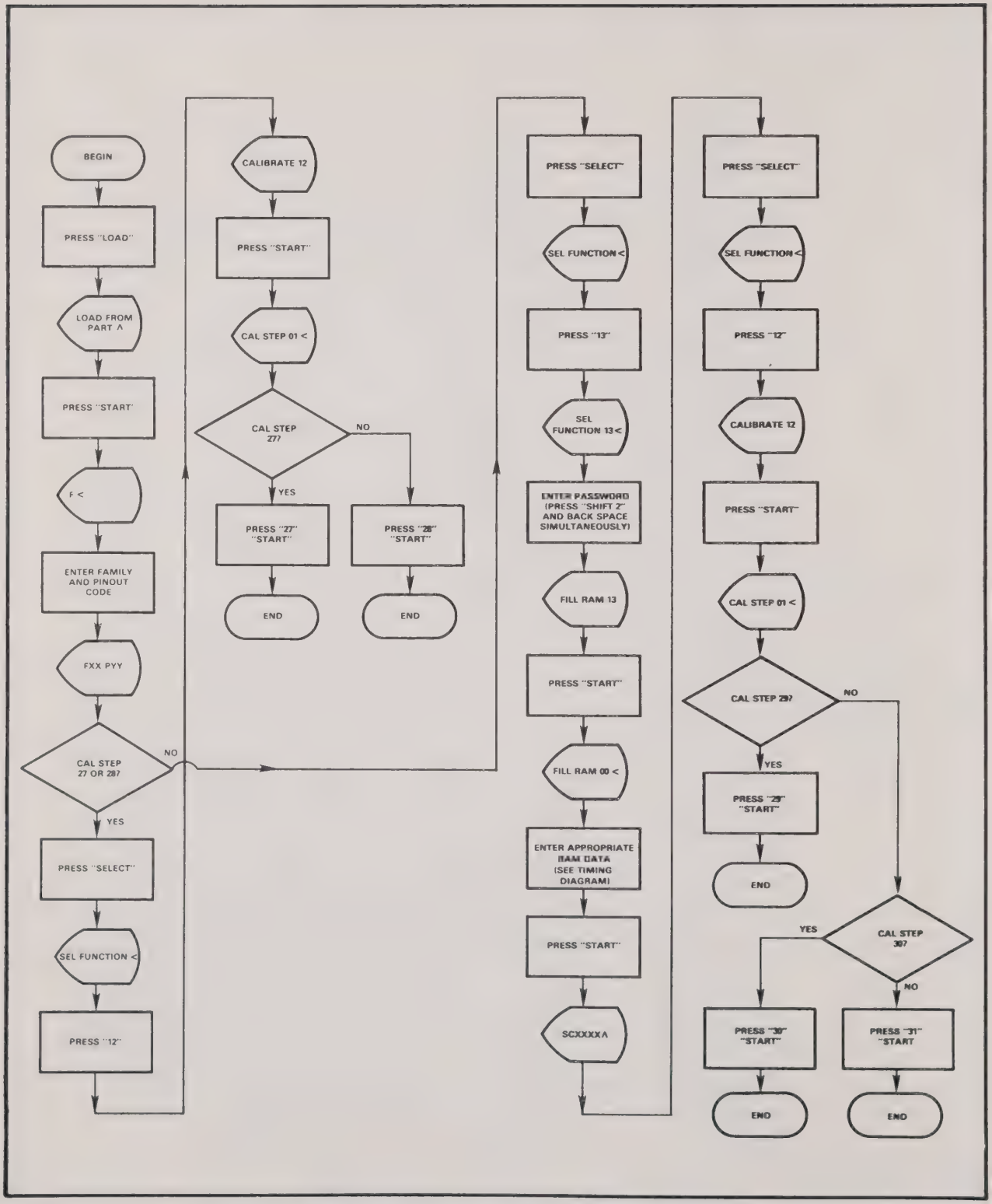

Figure 4-10. Accessing Calibration Steps 27, 28, 29, 30, 31 (Model 100A)

4.4.4 Detailed Explanation of the Timing Diagrams

This manual contains a timing diagram for each device family that can be programmed by the UniPak 2™. Each timing diagram contains a set of waveform photographs that show critical programming parameters. To use these diagrams and photographs, read the information provided below and refer to the sample timing diagram (figure 4-13).

1. FAMILY CODE NUMBER—corresponds to the family code number of the device (refer to table 1.2).

2. FAMILY CHARACTERISTIC TABLE—lists the minimum and maximum parameter values; voltage and timing parameters other than those listed in this table are to be considered non-critical with a ±10% tolerance.

3. NOTES—Important information pertaining to a timing diagram.

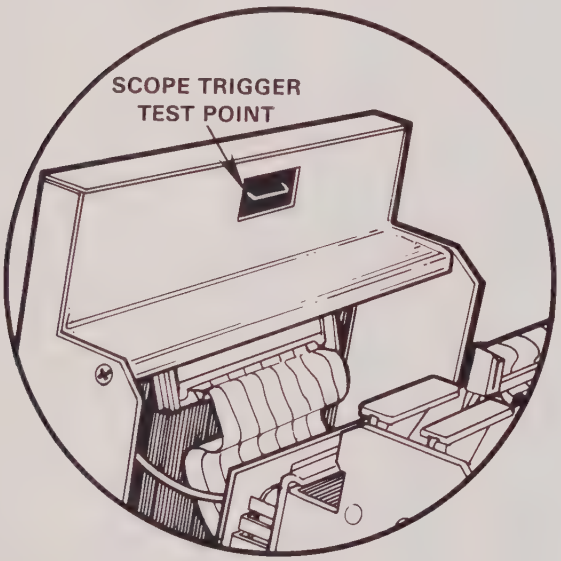

Figure 4-11. UniPak 2™ Scope Trigger Test Point

4. WAVEFORM NAMES—correspond to the pin names on the pinout chart (figure 4-12); the pinout chart tells you which socket pins to probe when you are observing the waveforms for a particular device pinout within a family. (The pinout is indicated by the number above each socket on figure 4-12 which corresponds to the pinout code on table 1.2.)

   We recommend that you use the oscilloscope's single sweep mode for address observation, since one trigger pulse is generated for each address change.

   - BIT NO PROG—always use the 02 (bit 2) contact (shown on figure 4-12)
   - BIT TO PROG—always use the 01 (bit 1) contact (shown on figure 4-12)

5. LAYOUT SEQUENCE NUMBER—used as a reference point within each diagram.

6. DELAY TIME POSITION—indicates the time from the start of the main sweep to the start of the delay time.

7. OSCILLOSCIPE GROUND REFERENCE—ground contact on the socket with its LED illuminated.

8. TIME-BASE AND VOLTS-PER-DIVISION SETTINGS—horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. The important observation is the timing relationship between the waveforms in the photographs. You can adjust this timing relationship on your oscilloscope to set convenient reference points. By taking into account any time-base variance, you can also make time comparisons between photographs. The time base is always the same for different waveforms in the same photograph.

9. EXPANDED PHOTOGRAPH NUMBER—corresponds to the photograph number. These detailed photographs are included to magnify rapid voltage changes or particular pulses in a pulse train.

10. VOLTAGE—indicates volts per division. The one in the upper left corner is for the top trace and the one in the lower left corner is for the bottom trace.

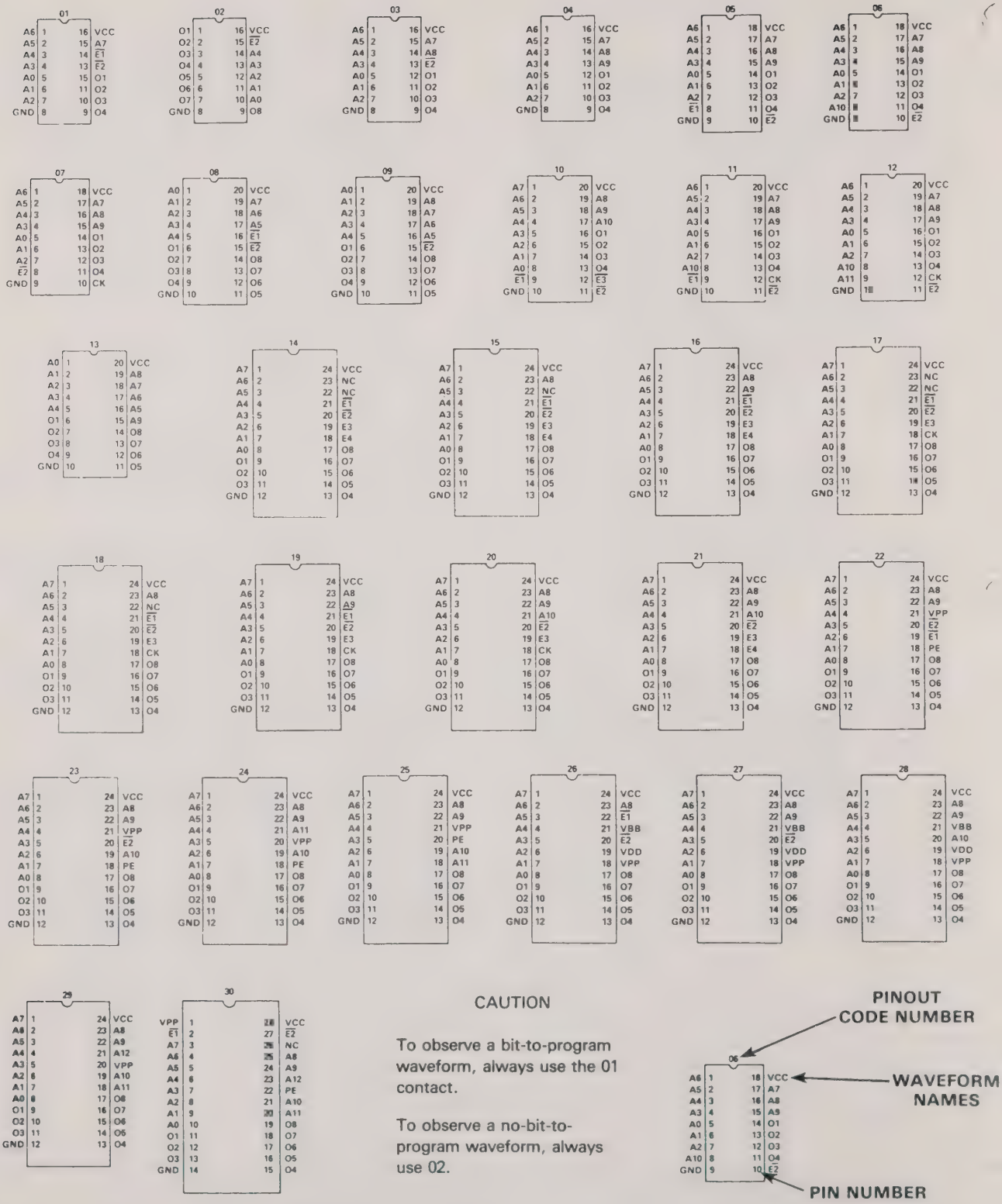

Figure 4-12. Pin Names by Pinout Code Numbers

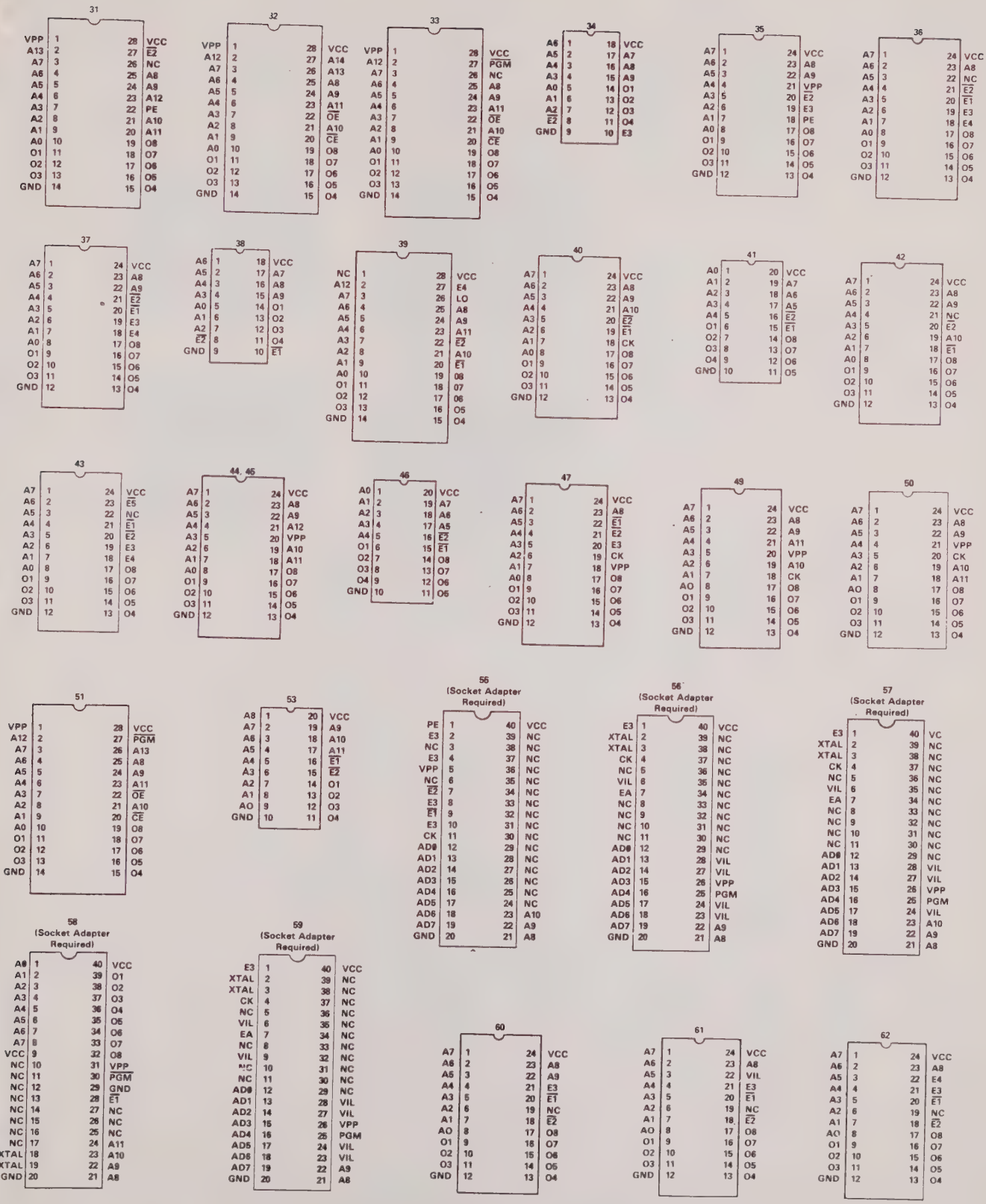

Figure 4-12. Continued

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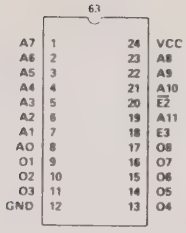

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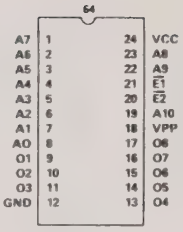

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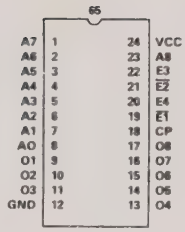

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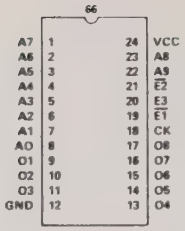

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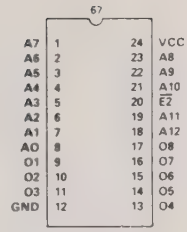

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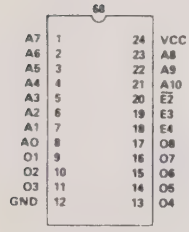

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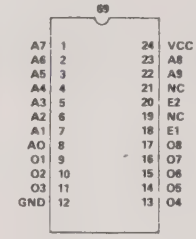

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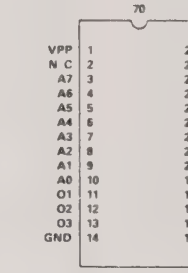

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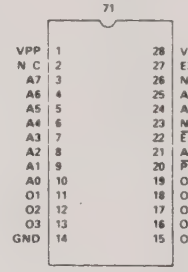

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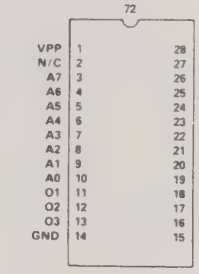

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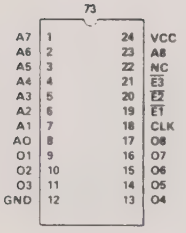

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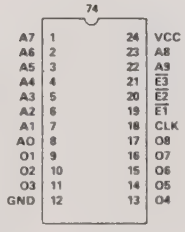

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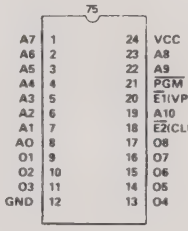

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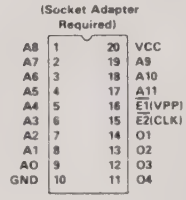

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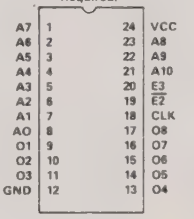

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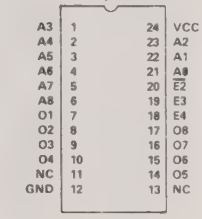

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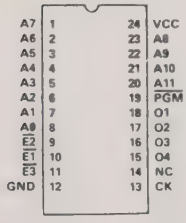

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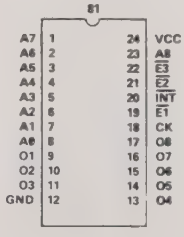

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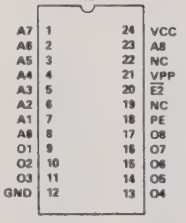

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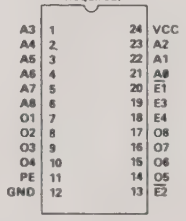

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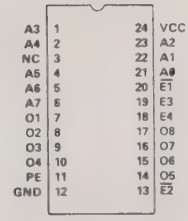

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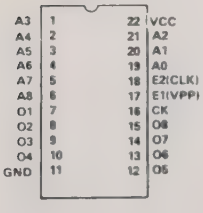

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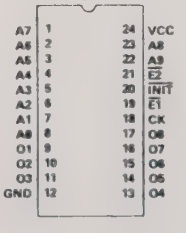

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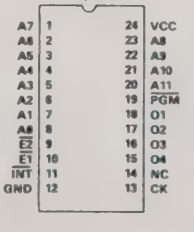

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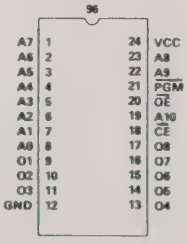

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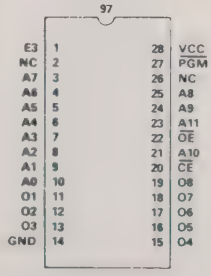


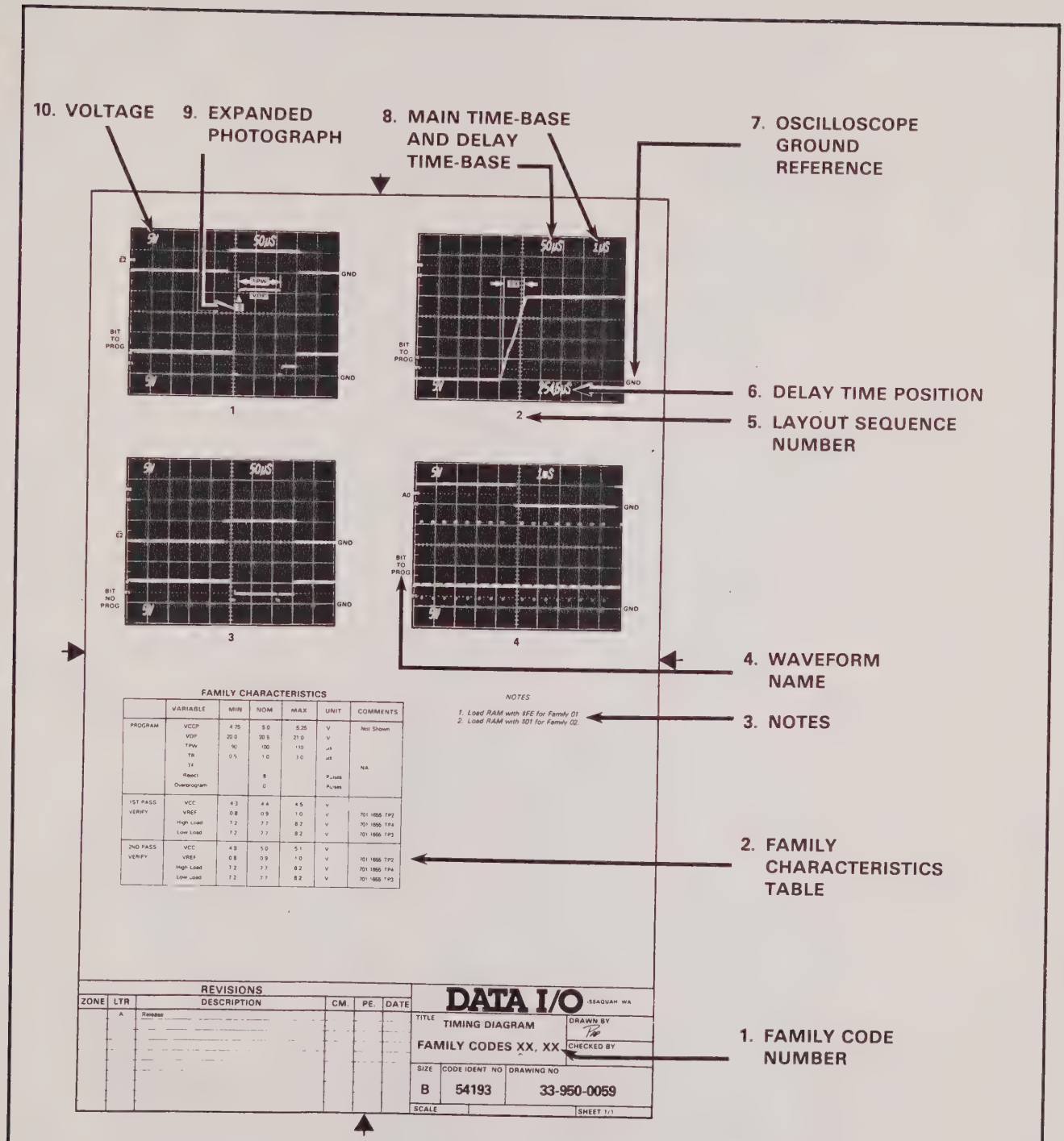


Figure 4-13. Sample Timing Diagram

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A		e.g.	10/82
C	ECN 4831	[illegible]	5/83

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
			The following tests are performed					
			with the UniPak 2™ on the calibration					
			extender.					
1	1	V reference supply	701-1655/TP2	14.4V	14.5V	14.6V	R8,701-1655	
	2	Load supply (high range)	701-1655/TP4	25.0V		26.0V		
	3	Load supply (low range)	701-1655/TP3	25.0V		26.0V		
	4	VCC supply	2 24	11.9V	12.0V	12.1V	R52,701-1690	
	5	CE supply	2 20	32.7V	33.0V	33.2V	R15,701-1690	
	6	Bit supply	2 9	25.7V	26.0V	26.2V	R31,701-1690	
	7	Address supply	2 8	14.8V	15.0V	15.2V	R28,702-1650	
2	8	V reference supply	701-1655/TP2	6.70V		6.90V		
	9	Load supply	701-1655/TP3	10.3V		11.7V		
3	10	V reference supply	701-1655/TP2	3.30V		3.50V		
	11	Current source 20mA	2 9	19.5mA	20.0mA	20.5mA	R3,702-1650	Use a 100 OHM, 2W carbon comp resistor in series with the current meter.
4	12	Current source supply	2 9	118mA	120mA	122mA	R2,702-1650	Use a 100 OHM, 2W carbon comp resistor in series with the current meter.

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A		C.J.3	10/82
C	ECN 4831	JH	5/83

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
5	13	Bit switch rise waveform	2 14				R1,701-1690	See waveform photograph (page 27).
6		DAC step waveforms						
	14	VCC	2 24					See waveform photograph (page 28).
	15	Bit supply	701-1690/TP2					
	16	CE supply	701-1690/TP1					
	17	VREF supply	701-1655/TP2					
	18	Load supply	701-1655/TP3					
			The following tests are performed					
			with the UniPak 2™ installed in its					
			normal operating position.					
7	19	Current DAC step waveform	2 9					Place a 200 OHM, 5W resistor
								between pins 9 and 12,
								socket 2 (page 26).
8	20	All voltages off	all all	-0.1V		0.4V		
9	21	Socket 2 LED						Confirm that socket 2 LED is on.
	22	VCC supply load	2 24	11.8V		12.1V		Place a 20 OHM, 2W resistor
								between pins 24 and 12,socket 2.
10	23	Fast VCC supply load	2 24	12.0V		13.0V		Same as above.

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A		E.J.J.	10/82
C	ECN 4831	JA	5/83

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
11	24	CE supply load	2 20	32.3V		33.2V		Place a 100 OHM, 10W resistor
								between pins 20 and 12,socket 2.
	25	Pin 18 voltage switch	2 18	32.7V		33.2V		
	26	Pin 21 voltage switch	2 21	32.7V		33.2V		
12	27	Bit supply load	2 11	25.2V		26.0V		Place a 100 OHM, 5W resistor
								between pins 11 and 12,socket 2.
	28	Pin 19 voltage switch	2 19	25.6V		26.2V		
13	29	VCC voltage linearity	2 24	3.90V		4.10V		
	30	CE supply linearity	2 18	23.0V		23.5V		Place a 2.2K OHM, 1/2W resistor
								between pin 12 and 18,
								socket 2.
	31	Address supply	2 8	4.70V		5.30V		
	32	-5V supply	2 21	-5.2V		-4.8V		
	33	12 volt supply	2 20	11.4V		12.6V		
	34	Clamp supply	2 11	20.5V		21.5V		
	35	Current source linearity	2 11	88mA		92mA		Use a 100 OHM, 2W carbon
								comp resistor in series with
								the current meter.
14	36	VCC voltage linearity	2 24	4.90V		5.10V		

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A		C.J.Z.	10/82
C	ECN 4831	[illegible]	5/83

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
	37	CE supply linearity	2 21	11.4V		12.0V		
	38	Clamp supply linearity	2 9	6.7V		7.3V		
15	39	VCC voltage linearity	2 24	5.90V		6.10V		
	40	I source and pulldowns	2 9,11,14,16	2.0V		2.6V		
	41	I source and pulldowns	2 10,13,15,17	0.0V		1.0V		
16	42	I source and pulldowns	2 10,13,15,17	2.0V		2.6V		
	43	I source and pulldowns	2 9, 11, 14, 16	0.0V		1.0V		
17	44	Socket 1 LED						Confirm that socket 1 LED is on.
	45	VCC voltage supply	1 28	4.90V		5.10V		
	46	Odd address and data	1 2,3,5,7,9,11,13,16,18,	4.5V		5.5V		
		high	20,22,24					
	47	Even address and data	1 4,6,8,10,12,15,17,19,21,	-0.1V		0.4V		
		low	23,25,27					
18	48	Odd address and data	1 2,3,5,7,9,11,13,16,18,	-0.1V		0.4V		
		low	20,22,24					
	49	Even address and data	1 4,6,8,10,12,15,17,19,21,	4.5V		5.5V		
		high	23,25,27					
19	50	Odd data lines high	1 11,13,16,18	25.5V		26.5V		
	51	Even data lines pullups	1 12,15,17,19	4.5V		5.5V		

Sheet 4 of 6

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A		C.J.3	10/82
C	ECN 4831	JH	5/83

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
20	52	Odd data lines pullups	1 11,13,16,18	4.5V		5.5V		
	53	Even data lines high	1 12,15,17,19	25.5V		26.5V		
21	54	Socket 3 LED						Confirm that socket 3 LED is on.
	55	VCC voltage supply	3 20	4.90V		5.10V		
22	56	Socket 4 LED						Confirm that socket 4 LED is on.
	57	VCC voltage supply	4 16	4.90V		5.10V		
23	58	Socket 5 LED						Confirm that socket 5 LED is on.
	59	VCC voltage supply	5 16	4.90V		5.10V		
24	60	Socket 6 LED						Confirm that socket 6 LED is on.
	61	VCC voltage supply	6 18	4.90V		5.10V		
25	62	Socket 7 LED						Confirm that socket 7 LED is on.
	63	VCC voltage supply	7 20	4.90V		5.10V		
26	64	VCC pullup 1 on	1 28	4.0V		5.2V		
		VCC pullup 2 on	2 24	4.0V		5.2V		
		VCC pullup 3 on	3 20	4.0V		5.2V		
		VCC pullup 4 on	4 16	4.0V		5.2V		
		VCC pullup 5 on	5 16	4.0V		5.2V		
		VCC pullup 6 on	6 18	4.0V		5.2V		
		VCC pullup 7 on	7 20	4.0V		5.2V		

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A		C.J.J.	10/82
C	ECN 4831	[illegible]	5/83

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
			Steps 25 through 31 are optional.					
27	65	Static 1st pass verify						See family characteristics table
		levels						in the applicable timing
								diagram.
28	66	Static 2nd pass verify						See applicable timing diagram.
		levels						
29	67	Programming waveforms						See applicable timing diagram.
30	68	Chip erase waveforms						See applicable timing diagram.
								For electrically eraseable
								devices only.
31	69	Byte erase waveforms						See applicable timing diagram.
								For electrically eraseable
								devices only.

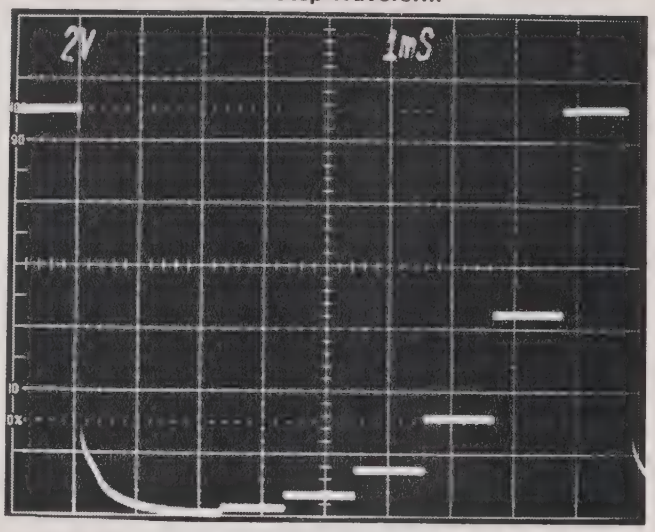
Sheet 6 of 6

Measurement Chart Photographs

Measurement Chart

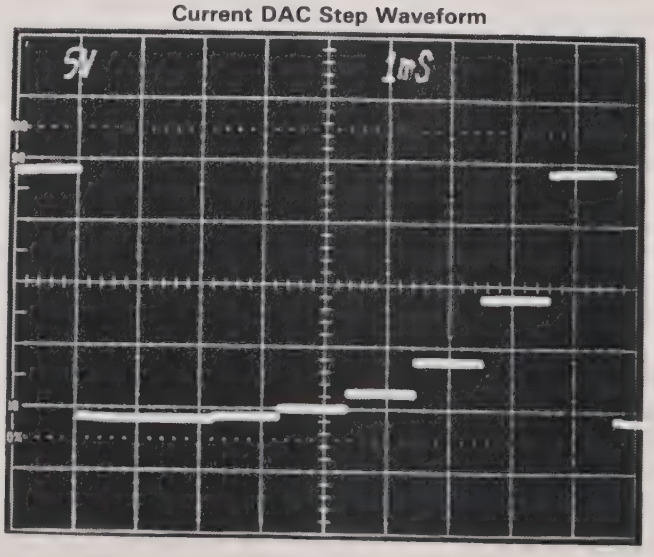
PROGRAM ELECTRONICS UNIPAK 2™

DAC Step Waveform



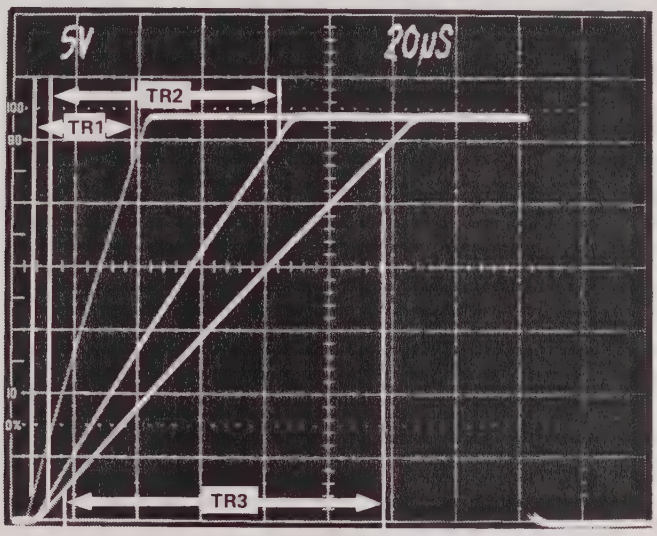
LOAD SUPPLY DAC

Current DAC Step Waveform



DATE	REV	REVISION RECORD	DR	CK
10-82	A			C.J.J.

Bit Switch Rise Waveform



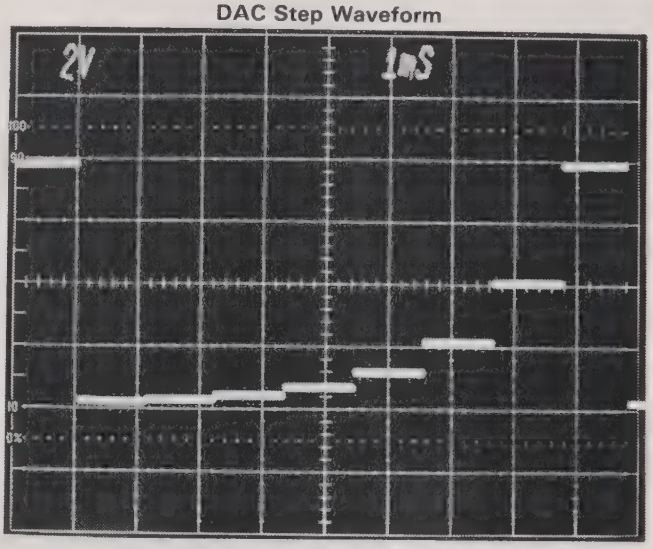
	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	TR1	29	33	37	us	
	TR2	65	66	67	us	Adjust R1, 701-1690
	TR3	90	100	110	us	

NOTE: All TR's are measured from 10% to 90%.

Measurement Chart

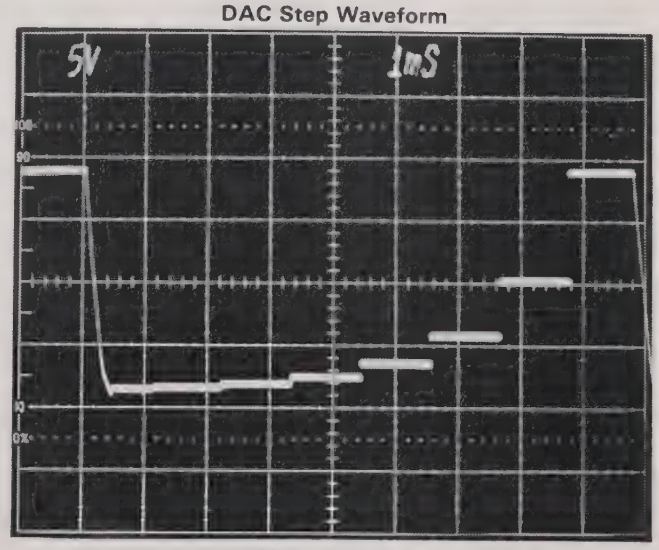
PROGRAM ELECTRONICS UNIPAK 2™

DAC Step Waveform



V_{CC} DAC

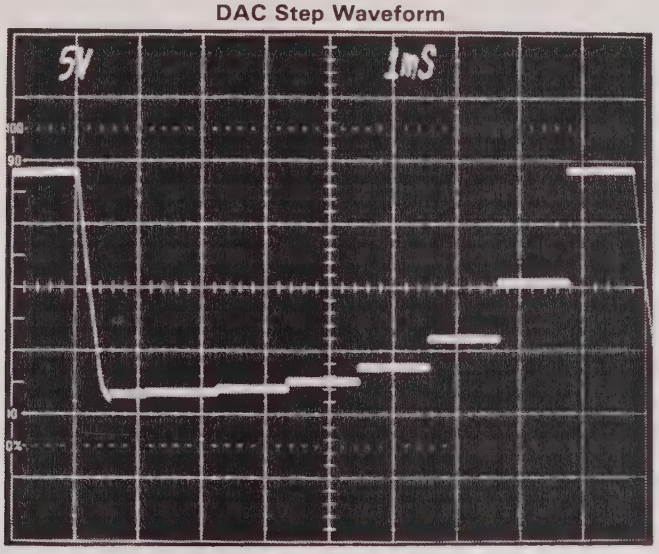
DAC Step Waveform



$\overline{CE}$ SUPPLY DAC

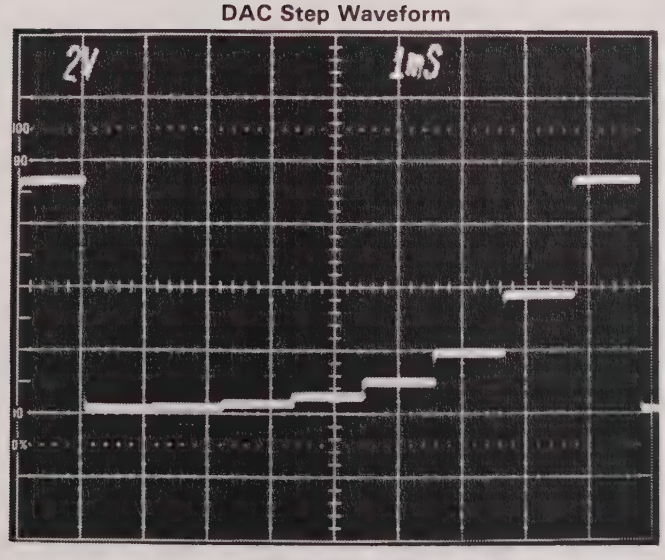
DATE	REV	REVISION RECORD	DR	CK
10-82	A			C.J.B.

DAC Step Waveform



BIT SUPPLY DAC

DAC Step Waveform



VREF SUPPLY DAC

SECTION 5
CIRCUIT DESCRIPTION

5.1 OVERVIEW

This section defines the functions of the UniPak 2™'s principal hardware components. Each circuit card assembly is depicted by a block diagram accompanied by a written description.

5.2 GENERAL ARCHITECTURE

5.2.1 The Link Between the UniPak 2™ and the Programmer

The UniPak 2™ is controlled by the programmer's extended processor bus through the UniPak 2™'s mating connector (J1). The control software for the UniPak 2™ is located in EPROM on the memory card (702-1650).

5.2.2 The Buses

The programmer's address bus, data bus, R/$\overline{W}$ line and $\overline{V \bullet \emptyset_2}$ line access the software on the memory card and control the gates and registers on the waveform generator (701-1690) and address cards (701-1655). The UniPak 2™'s device bus gathers the programming waveforms produced by these cards and transmits them to the socket card (702-1659). Figure 5-1 shows the relationships between the buses.

5.3 COMPONENT LAYOUT

The principal components of the UniPak 2™ are the motherboard, the waveform generator, the address card, the socket card, and the memory card. The component layout of the UniPak 2™ is shown in figure 5-2 and described in the following subsections.

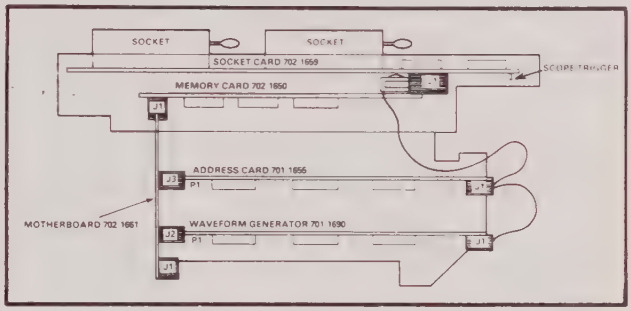


Figure 5-2. Principal Components

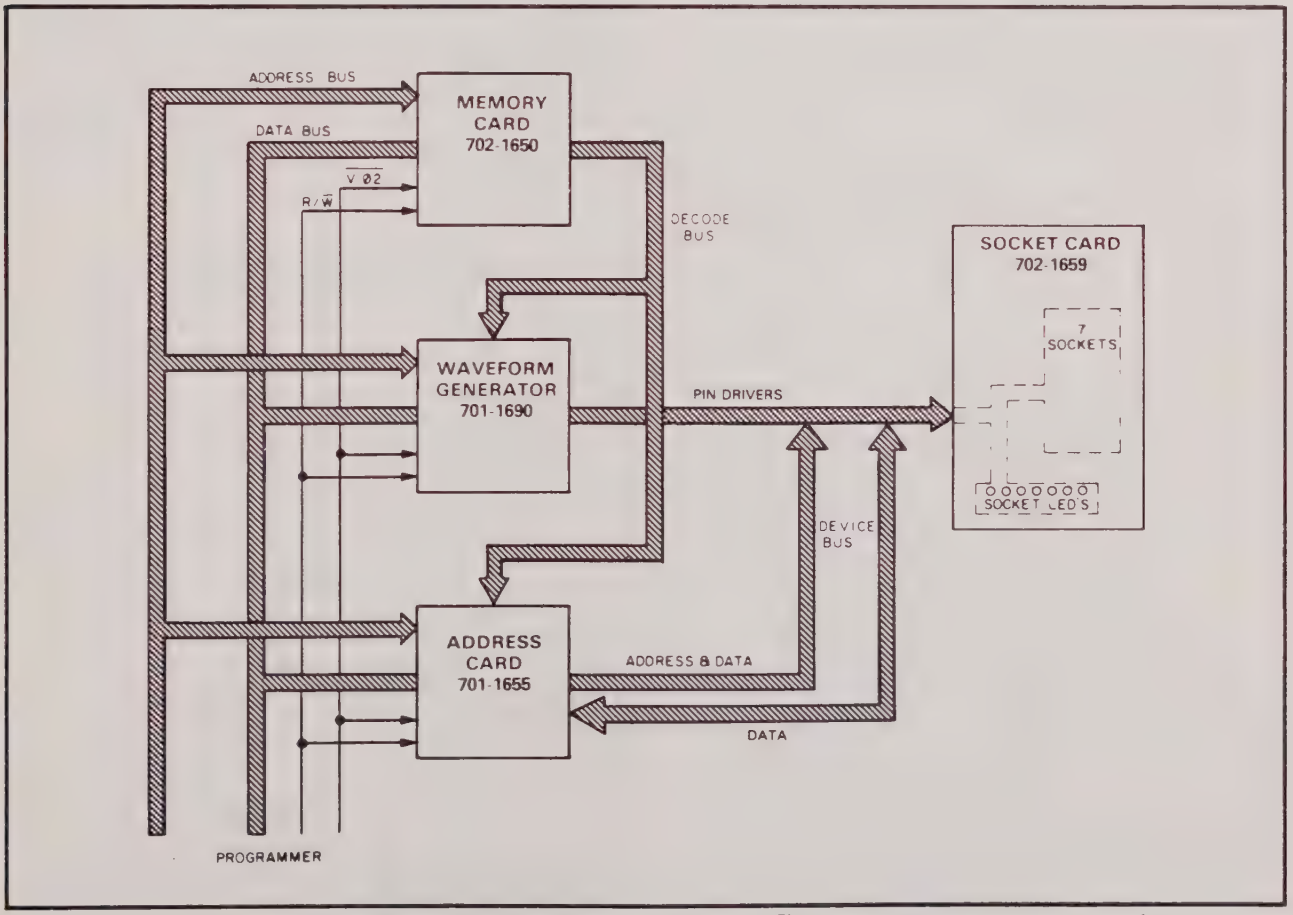


Figure 5-1. Block Diagram, UniPak 2™ Electronics

5.3.1 Motherboard

The motherboard accepts the signals and power supplies from the programmer and transmits them to two identical 72-pin edge connectors and a 50-pin edge connector; see figure 5-3 and schematic 30-702-1661.

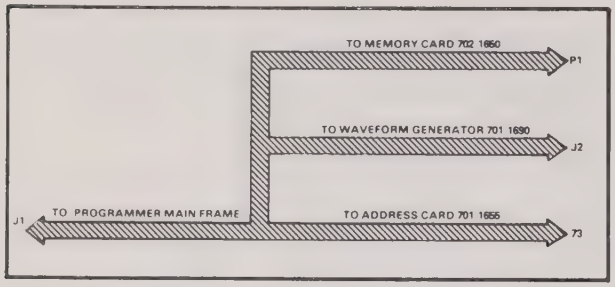


Figure 5-3. Block Diagram, Motherboard

5.3.2 Waveform Generator

The waveform generator provides signals required for programming devices. These signals are generated by the blocks shown in figure 5-4.

Three major supplies are the V_{CC} supply, the $\overline{CE}$ supply and the bit supply, which are used to generate the respective signals. Each supply is software-controlled via a D/A converter. All D/A converters obtain their reference voltage from the DAC reference.

The V_{CC} waveforms are generated by writing appropriate DAC values from the firmware. The rise and fall times are fixed by the slewing rate of the op amp. Two overcurrent detectors are included, one for low currents and one for high currents (above 1Amp). If a detector is activated, the control latch is reset; the DAC reference kill output then causes the DAC reference to go to zero, in turn causing all supplies to return to zero.

The V_{CC} supply senses the V_{CC} voltage at the PROM socket via the V_{CC} sense line. This remote sensing compensates for all cable drops between the supply and the socket.

The $\overline{CE}$ waveforms are generated by using the $\overline{CE}$ supply in conjunction with one of the pin switches. The voltage level is selected by writing the appropriate value to the $\overline{CE}$ DAC. One of two rise times is selected by the control latch and rise-time control circuitry. Either the pin 18, 20 or 21 switch can be enabled by the switch-control latch to output the high-level $\overline{CS}$ voltage. Switches that are not enabled can output TTL levels.

Each pin switch consists of an emitter follower with the collector tied to the $\overline{CE}$ supply. A current source is provided for the base of each switch to charge the common rise-time capacitor. When the base is released, a linear ramp is generated which is truncated at the $\overline{CE}$ supply level. An NPN-transistor pulldown is included in the switch to provide a 20V/µs controlled fall time. Logic circuitry prevents the pulldown and pullup circuits from being active simultaneously.

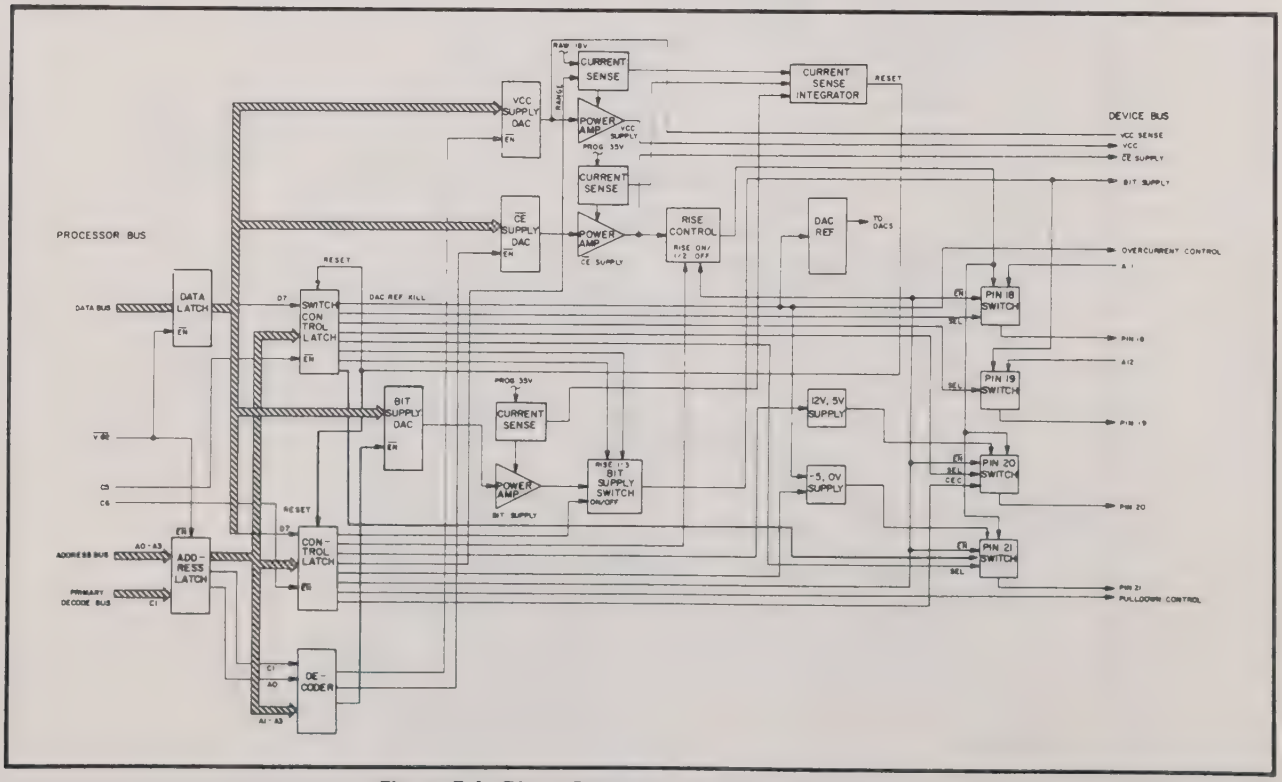


Figure 5-4. Block Diagram, Waveform Generator

The pin 21 switch uses the same principles as the pin 18 and pin 20 switches. However, a power amplifier output (0/-5V supply) provides the ground reference for the switch. For certain programming algorithms this amplifier output is brought to -5V.

The pin 20 switch includes a pullup that is connected to the +12/ +5V supply, thus allowing the switch in the TTL mode to switch from 0 to 12V as well as from 0 to 5V. The +12/ +5V supply consists of a monolithic regulator and a 5.1V zener diode controlled by the switch-control latch.

Signals to be applied to the data lines of a device are generated with the bit supply signals and controlled by the bit-supply switch. The bit supply is nearly identical to the $\overline{CE}$ supply but has one less diode in the feedback path compensating for one less drop in the switch paths. The bit-supply switch consists of an emitter follower, a current source, and three rise-time control capacitors. The collector of the emitter follower is connected to the bit supply; the base is connected to the current source and timing capacitor. The control latch can select the timing capacitor and also control the base of the switch. When the base is released, the output ramps linearly to the bit-supply level. The output on the bit-supply switch is sent to the address card and to the pin 19 switch; unlike the pin 20, 21 and 18 switches, the pin 19 switch consists of a simple PNP-saturating switch controlled by the switch-control latch.

The current-sense integrator smoothes the transient overcurrent pulses occurring from charging supply capacitors. When an overcurrent condition from the V_{CC}, $\overline{CE}$, bit or (0/-5V) supply exists for sufficient time, the control latch is reset, in turn causing the DAC reference and the supplies to go to zero. The state of the overcurrent-control line can be read by the address card and used by the programmer to detect shorted devices. Table 5-1 gives the functions of the device-bus pins. The data latch buffers the data bus and holds data to satisfy the long DAC data-hold requirement. The address latch buffers the lower-order address lines and the primary decode bus. These buffered lines are then sent to the decoder and the address latches. The decoder provides decode signals to the DACs for the V_{CC}, $\overline{CE}$ and bit supplies. The switch-control latch and the control latch receive their clocks from a decoder on the address card.

Table 5-1. Pin Functions, Device Bus (At J1)

Pin	Function	Pin	Function
1	PA_8	26	PA_7
2	PA_9	27	PA_6
3	PA_{10}	28	PA_5
4	PA_{11}	29	PA_4
5	PA_{12}	30	PA_3
6	PA_{13}	31	PA_2
7	PA_{14}	32	PA_1
8	PA_{15}	33	PA_0
9	GND	34	Vcc
10	Vcc Sense	35	GND
11	CE Supply	36	GND
12	Bit Switch	37	Bit Supply
13	Pin 20	38	Pin 18
14	Pin 21	39	Pin 19
15	Scope Trigger	40	PD_1
16	-9V	41	PD_2
17	+24V	42	PD_4
18	$\overline{\text{Overcurrent}}$	43	PD_8
19	$\overline{\text{Pull-Down Control}}$	44	S1
20	$\overline{\text{Vcc Pull-Up Control}}$	45	S2
21	Address Supply +5V Select	46	$\overline{\text{S3}}$
22	PD_8	47	$\overline{\text{Vcc Pulse}}$
23	PD_7	48	Address DAC
24	PD_6	49	+5V
25	PD_5	50	Bit Switch Control

5.3.3 Address Card

The address card, illustrated in figure 5-5, provides the device address, device data, data loads and supply measurement capability of the UniPak 2™.

The address drivers consist of addressable latches driving the device address bus. The addressable latches receive data from the most-significant-bit line of the data bus.

The data switch register drives PNP data switches which direct the output of the bit switch to the appropriate device-data line. The PNP switches are driven by current sources to provide a constant base drive at all bit-switch voltages.

The data sink register is used to shunt programming currents to ground. Device data is read via the data comparators and strobed to the processor bus via the data gate. The comparators receive their reference voltage from the V_{REF} amplifier which is controlled by the V_{REF} DAC. Loading the device data bus is controlled by the load DAC, the load amplifier and the high/low-range load switch. This supply develops a voltage that is applied to either the low-range or high- and low-range load resistor banks. These resistors are fed through isolation diodes which are connected to the device data pins. The load sink register enables the UniPak 2™ to select which device data pins will have loads applied to them. The diode clamps limit the voltage applied by the load resistors to the data bus to approximately 5V when the load clamp switch is closed.

The supply comparators read the V_{CC}-sense line, the $\overline{CE}$ supply and the bit switch line. The comparator gate/multiplexer strobes the data from the supply comparators or overcurrent-read line to the most significant bit line of the data bus.

The socket-select latch provides a control line for the high/low range switch and control lines for the socket card.

The data latch buffers the data bus and holds data to satisfy the DAC requirements.

The current source latch will supply a 4mA current to a device provided there is a 15V zener diode inside the device on pin 18, 19 or 20. The address supply 5V select determines whether the address supply DAC or a fixed 5V will be applied to PA0-PA3.

The address latch buffers low-order addresses for the secondary decoder. The secondary decoder provides the

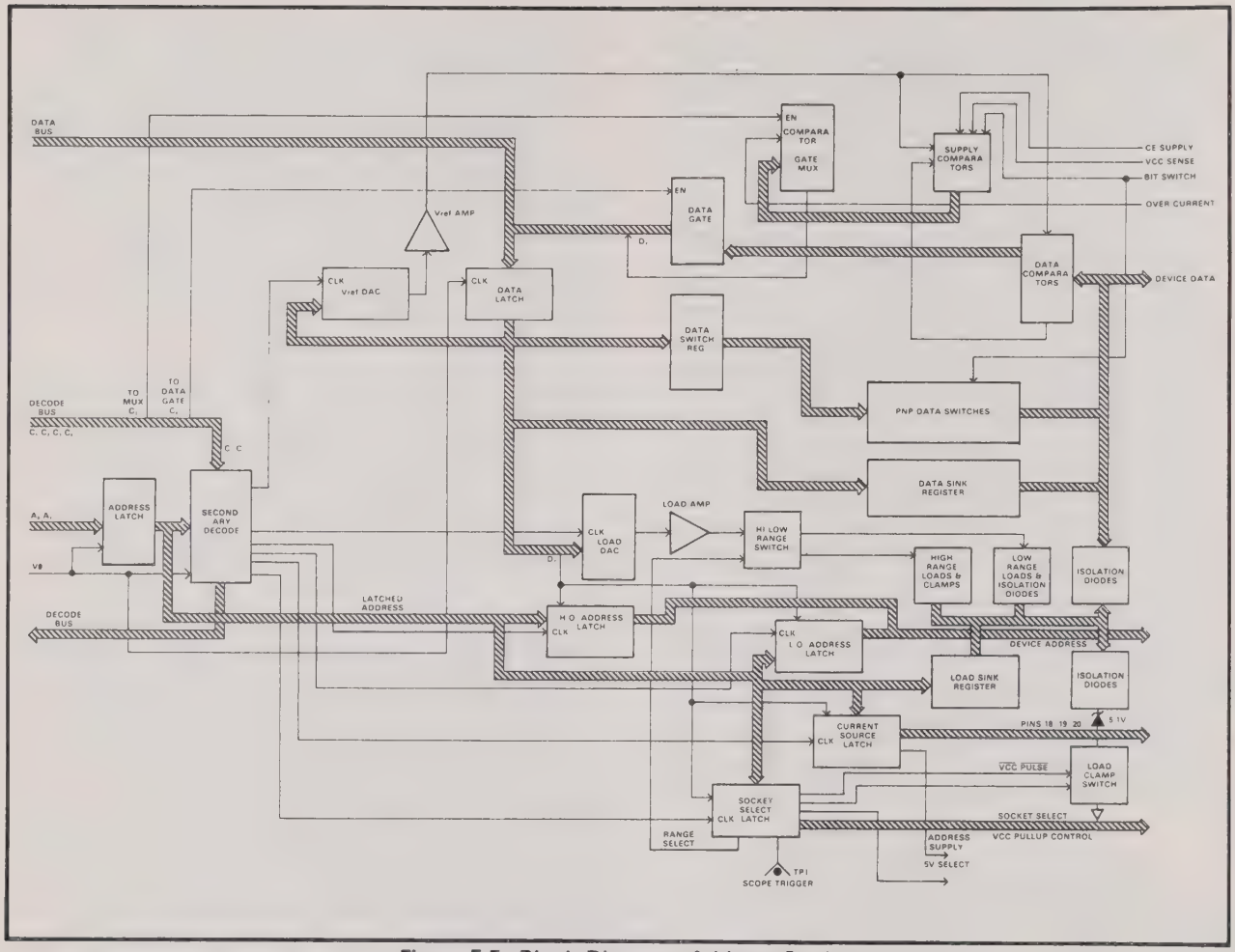


Figure 5-5. Block Diagram, Address Card

appropriate signals for the DACs and registers as well as the latches on this card and on the waveform generator. The $V \bullet \emptyset_2$ signal controls the timing of the various clock signals developed by the decoder.

5.3.4 Socket Card

The socket card distributes to the device sockets the signals developed on the address card and the waveform generator; refer to figure 5-6.

The device address bus (PA0-PA15) is generated on the address card and fed to the socket card via the ribbon cable. On the socket card the bus is fed into CMOS buffers. The address supply DAC connects to the V_{DD} supply on these buffers. This allows the VOH level to be under DAC control. The address supply 5V select line allows PA0-PA3 to switch at TTL levels while all other address lines switch between "0" and the address supply level. The address clamps provide overvoltage protection and are connected to a comparator that senses overvoltage, shutting down all the supplies when excessive voltage is detected.

The device-data bus connects directly to all sockets. Four-bit devices are connected to PD1-PD4. The data pulldowns consist of 1k resistors and a diode network. The data clamp has two modes of operation controlled by the bit switch control line.

When voltage pulses are being applied to a device the pass element of the data clamp is switched out of the circuit. The op amp and 2.2k resistor precharge the 0.1µF capacitors to the level set by the bit supply so that the network does not absorb energy from the actual data-line programming pulses.

When current pulses are being applied to a device the pass element is switched into the circuit. The data clamp will be set to a voltage level by the bit supply and will sink all unnecessary current.

Pins 18, 19, 20 and 21 of the 24-pin device socket receive signals directly from the waveform generator via the corresponding pin switches. A spike-suppression network is provided where the $\overline{CE}$ supply charges an R-C network. V_{CC} is applied to all sockets through seven diodes. Remote sensing of the voltage at the selected socket is provided by

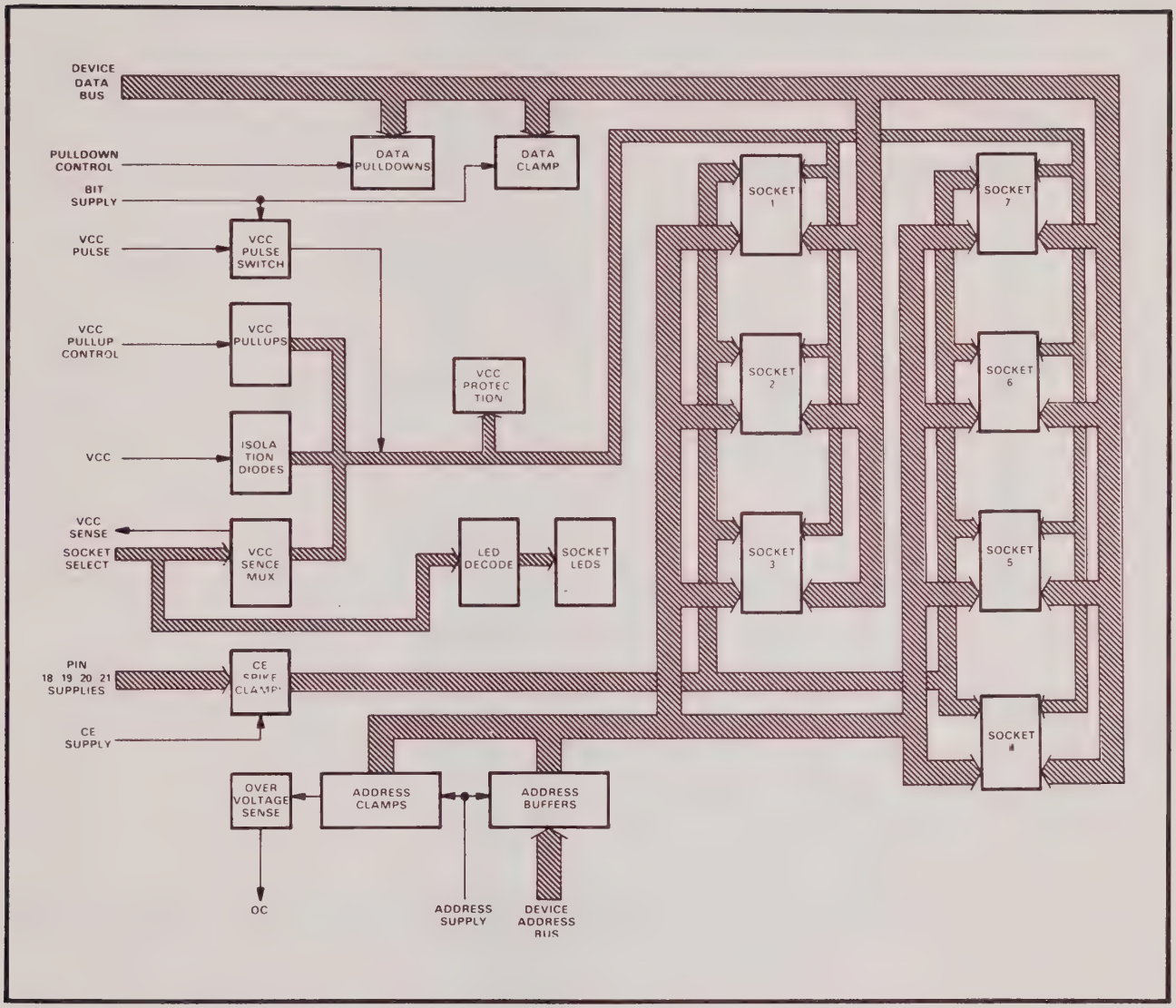


Figure 5-6. Block Diagram, Socket Card

the analog switch of the V_{CC}-sense multiplexer. When V_{CC} is brought to zero, the device's V_{CC} lines can be pulled high by the V_{CC} pullups. The V_{CC} sense-multiplexer and a comparator on the address card are then used to read the V_{CC} voltage. If a device is properly inserted in a socket the V_{CC} voltage will be above 2V. If it is in backwards it will be below 1V, and if no device is in the socket the voltage will approach 4V.

The V_{CC} pulse switch is used to switch from a level set by the V_{CC} supply to a level set by the bit supply. The switch uses a HEX FET with an RC network to control the rise and fall times. When the HEX FET is switched on, the V_{CC} isolation diode is reversed biased and the V_{CC} sense line sees a dummy load. The V_{CC} pulse switch is only applied to the 24-pin socket. When the switch is on, the .01µF decoupling capacitor for the 24-pin socket is switched off.

The LED decoder is used to light the LEDs below the selected socket.

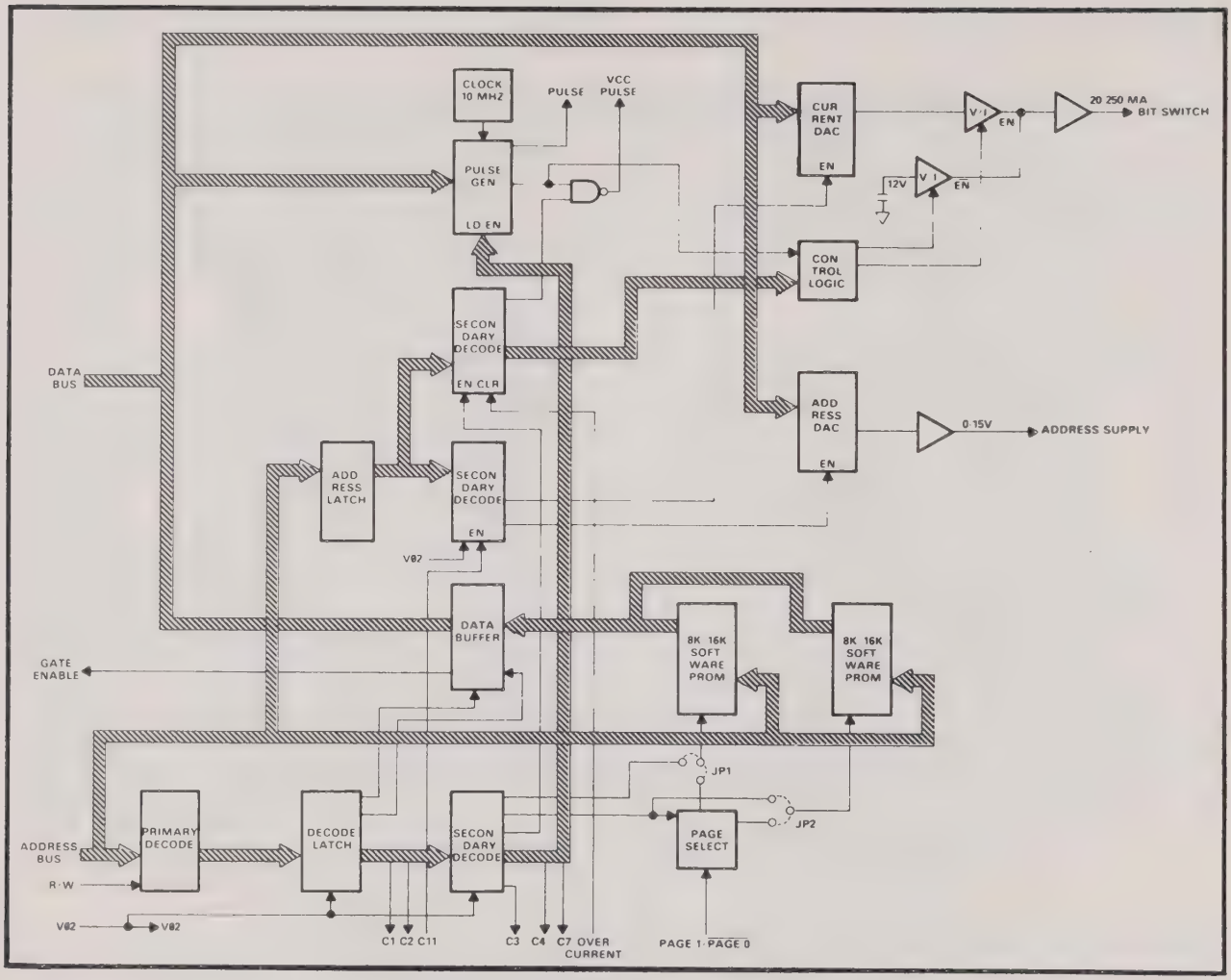


Figure 5-7. Block Diagram, Memory Card

5.3.5 Memory Card

The UniPak 2™ memory card is shown in figure 5-7. EPROMs which store the UniPak 2™ firmware are contained on the memory card. These EPROMs connect to the address bus directly and to the data bus through data buffers.

Paging is used when the 16k x 8 PROMs are installed. Two EPROMs and a latch comprise the primary decoding for the entire UniPak 2™. The EPROMs connect to the 12 high-order address lines and the R/$\overline{W}$ line. Outputs from the primary-decoder latch connect to the secondary decoder and also to secondary decoders on the address card and the waveform generator. A 1-of-8 decoder, timed with $\overline{V \bullet \emptyset_2}$, provides the secondary decoding for the software EPROMs. Two additional lines from this decoder connect to the address card to provide the decode signals for the data gate and comparator gate/multiplexer. Additional outputs from the binary decoder enable the data buffer during all software-read operations and lower the data gate enable line during any access of the UniPak 2™.

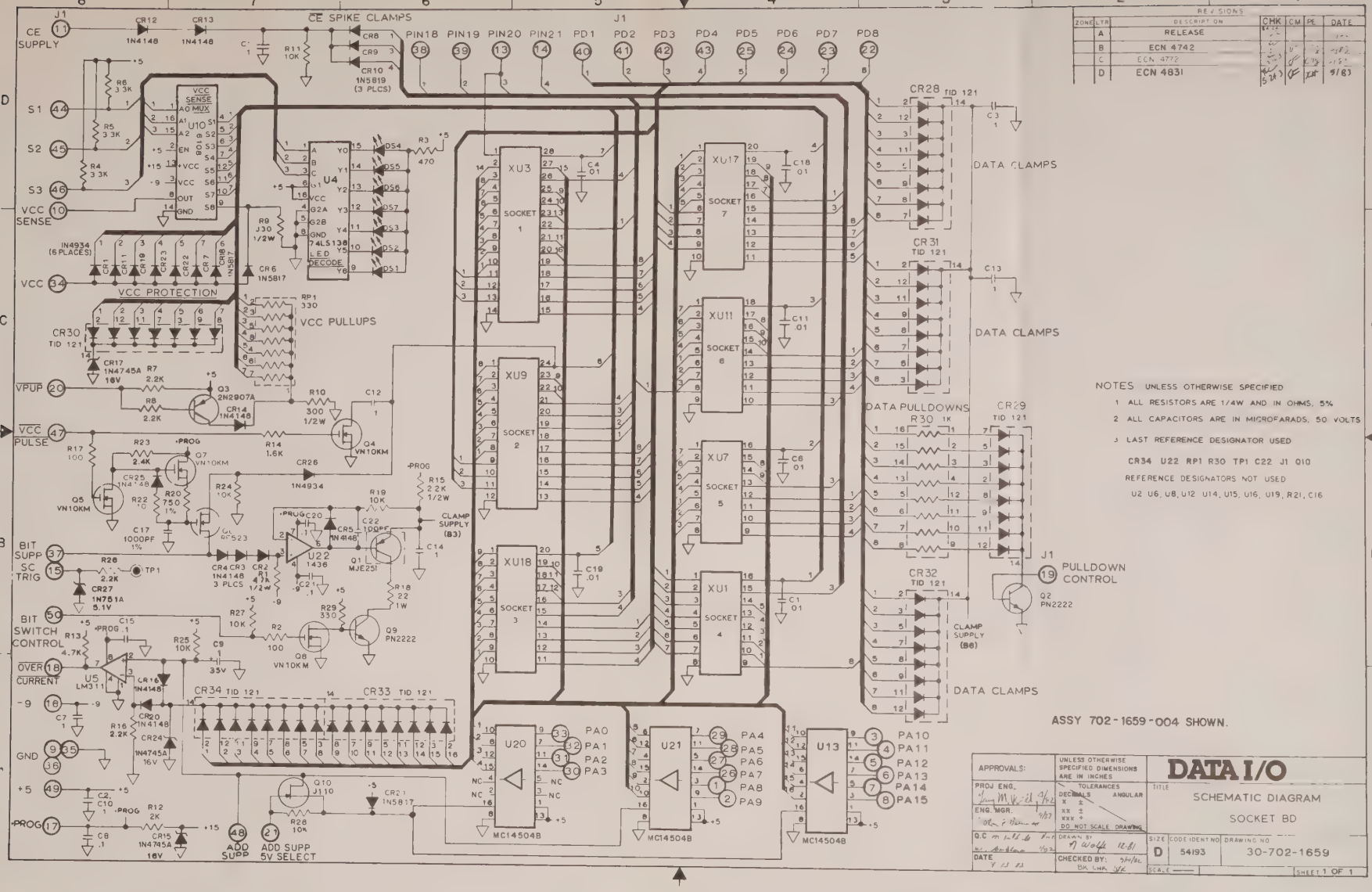
The pulse generator consists of a count-up ripple counter, an 8 bit latch, and a 10MHz crystal-controlled clock. The latch is connected to the data bus and is used to load the counter allowing the pulse generator to be programmable between 0.1 and 25.5µs.

The current source consists of a fixed 20mA current source and a programmable current source. The control logic selects which current source is active. The pulse generator can be selected to control the programmable current source.

The address supply generates the voltage necessary to drive the CMOS buffers located on the socket card. The voltage is generated from the 24V power supply using an NPN transistor driven by an op amp. The input of the op amp is a DAC which allows the voltage to be software-selectable.

SECTION 6
SCHEMATICS

30-702-1659	Socket Card
30-702-1650	Memory Card
30-701-1690	Waveform Generator
30-701-1655	Address Card
30-702-1661	Motherboard



ZONE	LTR	DESCRIPTION	CHK	CM	PE	DATE
	A	RELEASE				
	B	ECN 4742				
	C	ECN 4772				
	D	ECN 4831				9/83

NOTES UNLESS OTHERWISE SPECIFIED

1 ALL RESISTORS ARE 1/4W AND IN OHMS, 5%

2 ALL CAPACITORS ARE IN MICROFARADS, 50 VOLTS

3 LAST REFERENCE DESIGNATOR USED

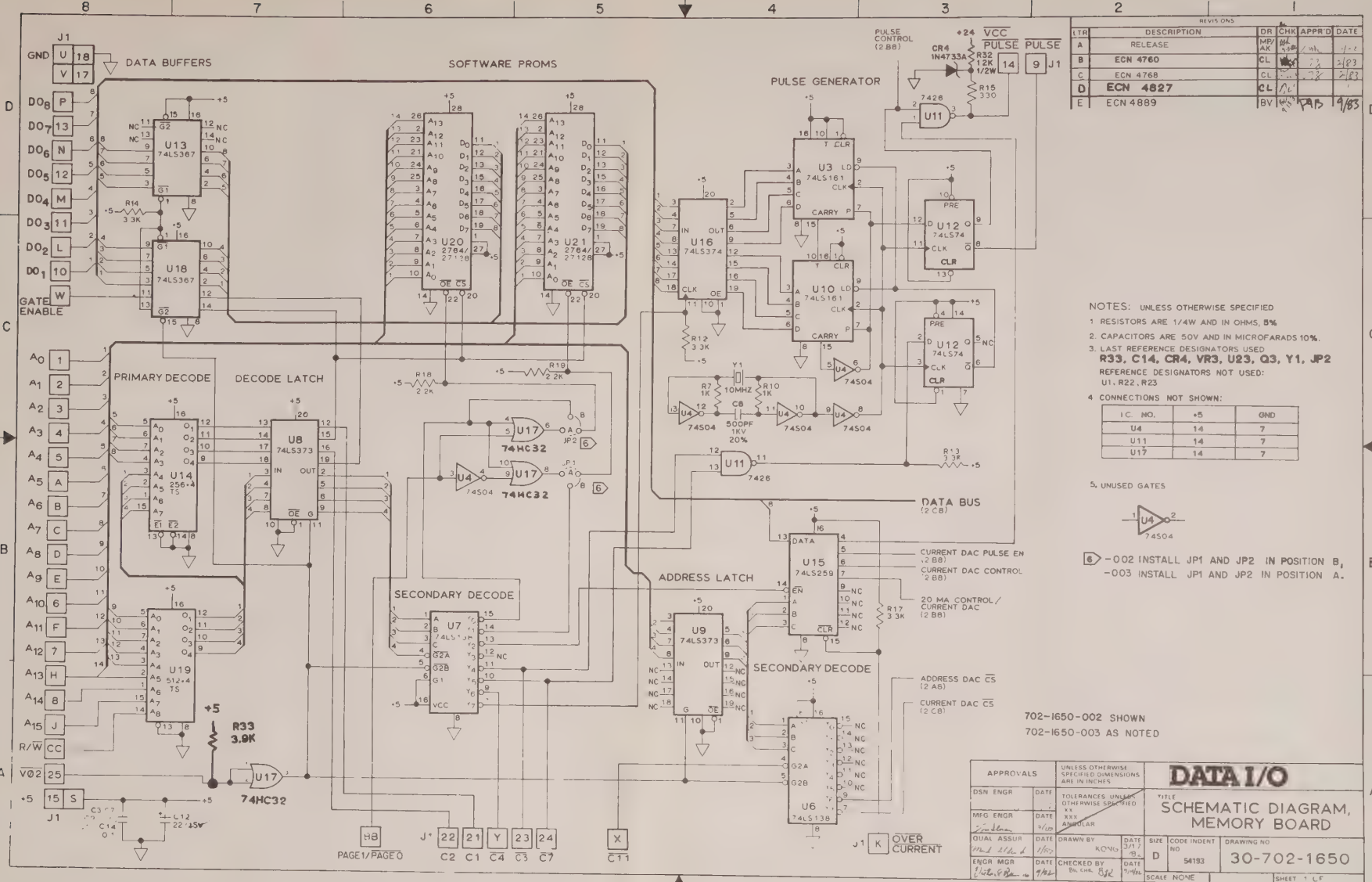
CR34 U22 RP1 R30 TP1 C22 J1 Q10

REFERENCE DESIGNATORS NOT USED

U2 U6, U8, U12 U14, U15, U16, U19, R21, C16

ASSY 702-1659-004 SHOWN.

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ ENG.	TOLERANCES DECIMALS ANGULAR	TITLE	SCHEMATIC DIAGRAM
ENG. MGR.	DO NOT SCALE DRAWING		SOCKET BD
Q.C.	DRAWN BY: M Wolfe 12-81	SIZE D	CODE IDENT NO 54193
DATE	CHECKED BY: BK CHA WK	SCALE	DRAWING NO 30-702-1659
			SHEET 1 OF 1



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP/AK	[illegible]	[illegible]	4-82
B	ECN 4760	CL	[illegible]	[illegible]	2/83
C	ECN 4768	CL	[illegible]	[illegible]	2/83
D	ECN 4827	CL	[illegible]	[illegible]	[illegible]
E	ECN 4889	BV	[illegible]	PAB	9/83

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 1/4W AND IN OHMS, 5%
2. CAPACITORS ARE 50V AND IN MICROFARADS 10%.
3. LAST REFERENCE DESIGNATORS USED
   R33, C14, CR4, VR3, U23, Q3, Y1, JP2
   REFERENCE DESIGNATORS NOT USED:
   U1, R22, R23
4. CONNECTIONS NOT SHOWN:

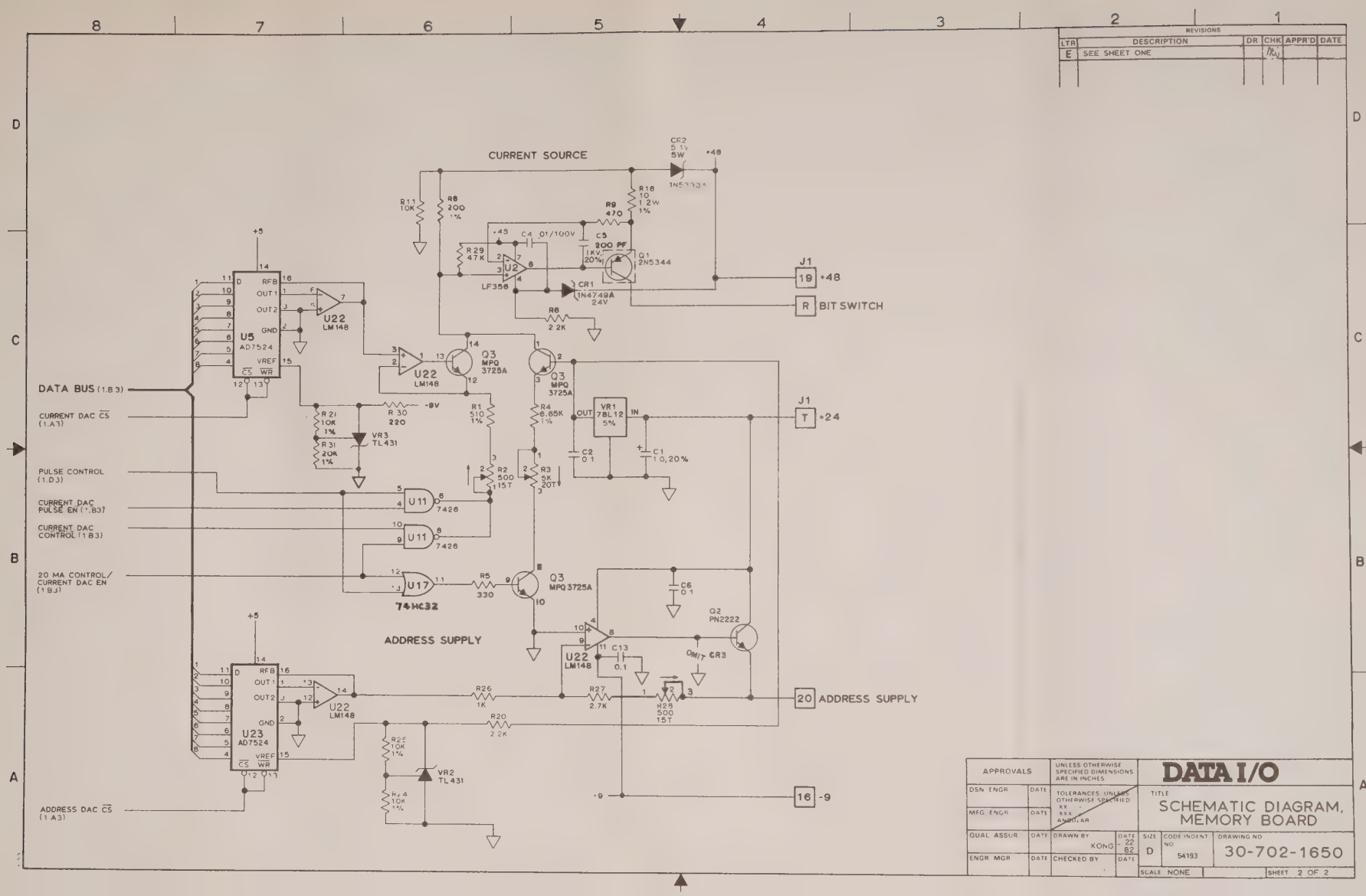
I.C. NO.	+5	GND
U4	14	7
U11	14	7
U17	14	7

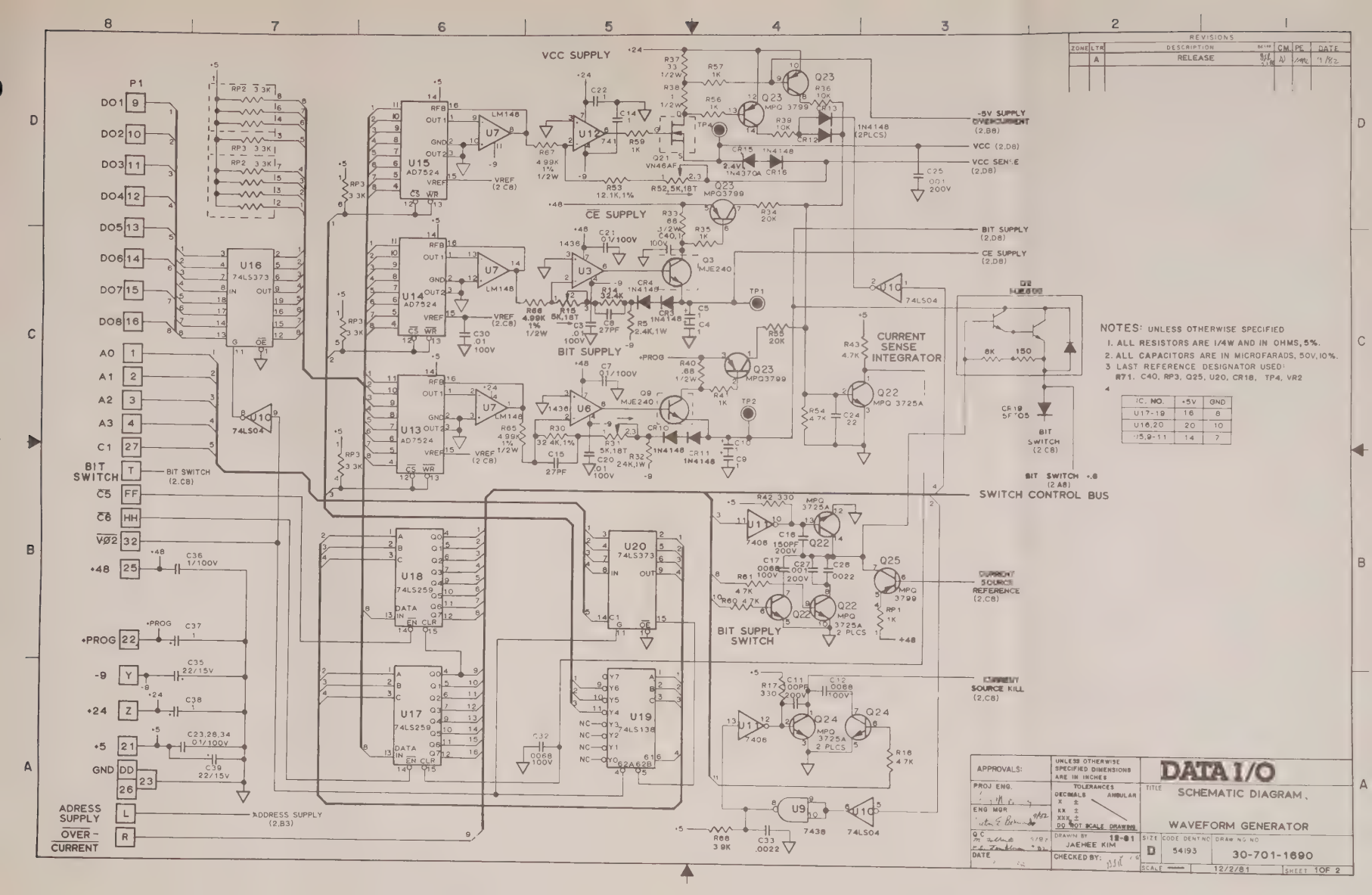
5. UNUSED GATES

6 -002 INSTALL JP1 AND JP2 IN POSITION B,
-003 INSTALL JP1 AND JP2 IN POSITION A.

702-1650-002 SHOWN
702-1650-003 AS NOTED

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED: XX ±.01, XXX ±.005, ANGULAR	TITLE: SCHEMATIC DIAGRAM, MEMORY BOARD	
MFG ENGR	DATE 9/19			
QUAL ASSUR	DATE 1/83	DRAWN BY: KONG	DATE 3/17/83	SIZE: D
ENGR MGR	DATE 9/82	CHECKED BY: [illegible]	DATE 9/19/83	CODE IDENT NO: 54193
				DRAWING NO: 30-702-1650
				SCALE: NONE
				SHEET 1 OF


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE
CURRENT SOURCE
CR2 5.1V 5W
+48
1N5333A
R11 10K
R8 200 1%
R9 470
R16 10 1/2W 1%
C4 .01/100V
C5 200 PF 1KV 20%
R29 47K
U2 LF356
Q1 2N5344
CR1 1N4749A 24V
R6 2.2K
J1 19 +48
R BIT SWITCH
+5
U5 AD7524
RFB OUT1 OUT2 GND VREF CS WR
U22 LM148
DATA BUS (1,B3)
CURRENT DAC CS (1,A3)
R21 10K 1%
R31 20K 1%
R30 220
-9V
VR3 TL431
Q3 MPQ 3725A
R1 510 1%
R4 6.65K 1%
VR1 78L12 5%
OUT IN
J1 T +24
C2 0.1
C1 10, 20%
R2 500 15T
R3 5K 20T
PULSE CONTROL (1,D3)
CURRENT DAC PULSE EN (1,B3)
CURRENT DAC CONTROL (1,B3)
U11 7426
20 MA CONTROL/ CURRENT DAC EN (1,B3)
U17 74HC32
R5 330
C6 0.1
Q2 PN2222
ADDRESS SUPPLY
U22 LM148
C13 0.1
OMIT CR3
U23 AD7524
R26 1K
R27 2.7K
R28 500 15T
20 ADDRESS SUPPLY
R20 2.2K
R25 10K 1%
R24 10K 1%
VR2 TL431
-9
16 -9
ADDRESS DAC CS (1,A3)
APPROVALS
DSN ENGR DATE
MFG ENGR DATE
QUAL ASSUR DATE
ENGR MGR DATE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR
DRAWN BY KONG DATE 2-22-82
CHECKED BY DATE
DATA I/O
TITLE SCHEMATIC DIAGRAM, MEMORY BOARD
SIZE D CODE IDENT NO 54193 DRAWING NO 30-702-1650
SCALE NONE SHEET 2 OF 2

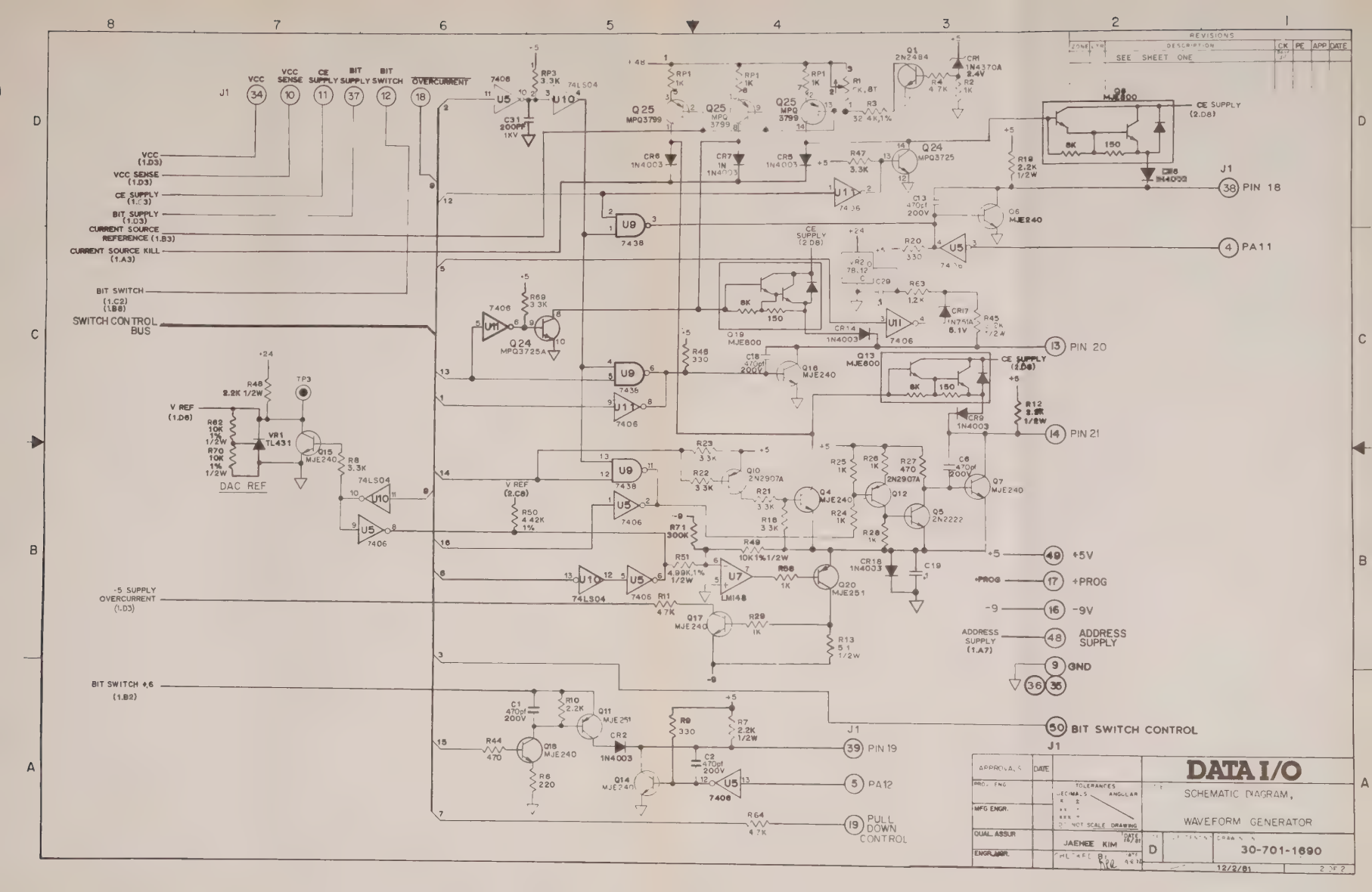


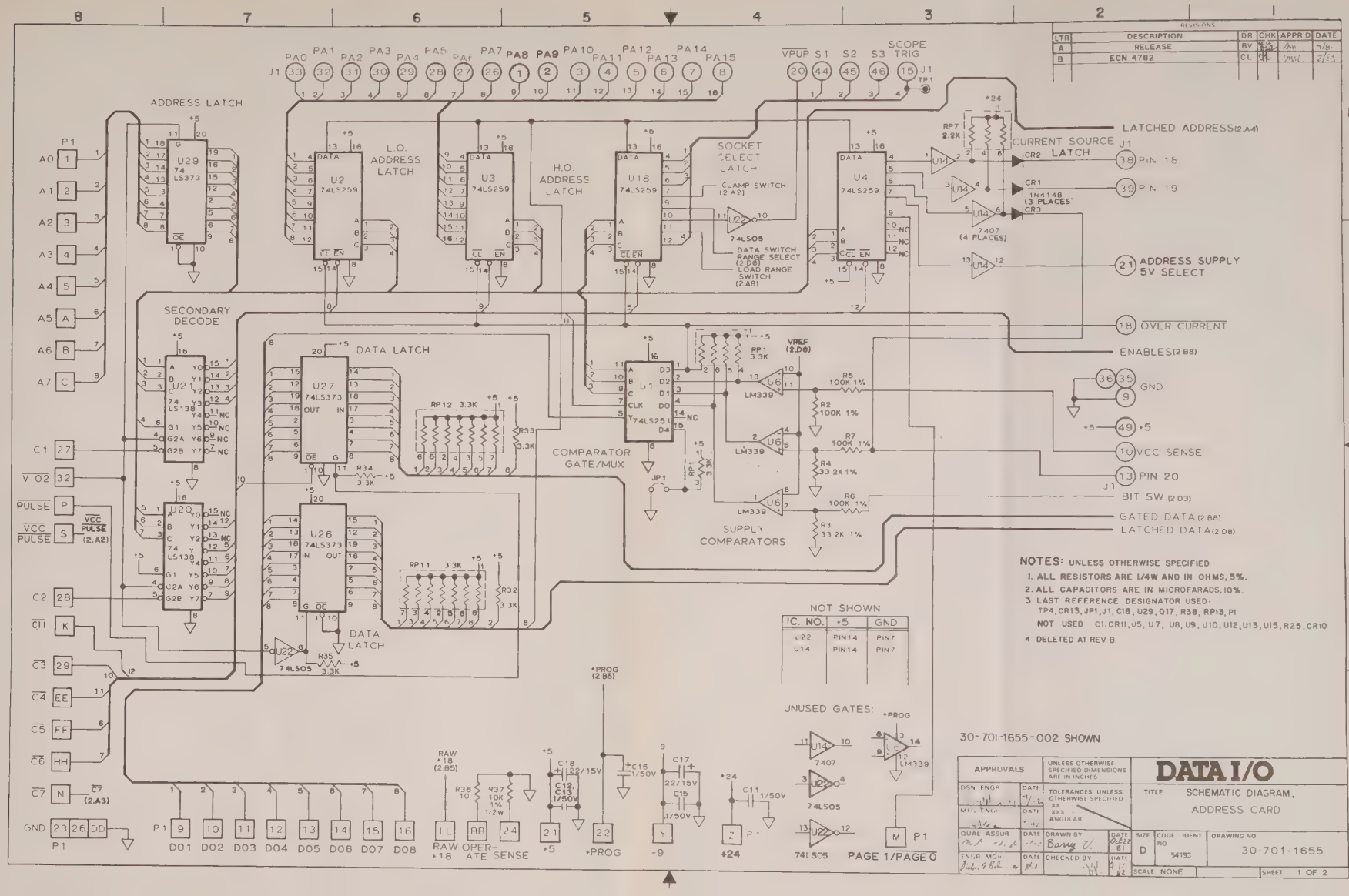
REVISIONS					
ZONE	LTR	DESCRIPTION	CM	PE	DATE
	A	RELEASE			9/82

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V, 10%.
3 LAST REFERENCE DESIGNATOR USED:
R71, C40, RP3, Q25, U20, CR18, TP4, VR2
4

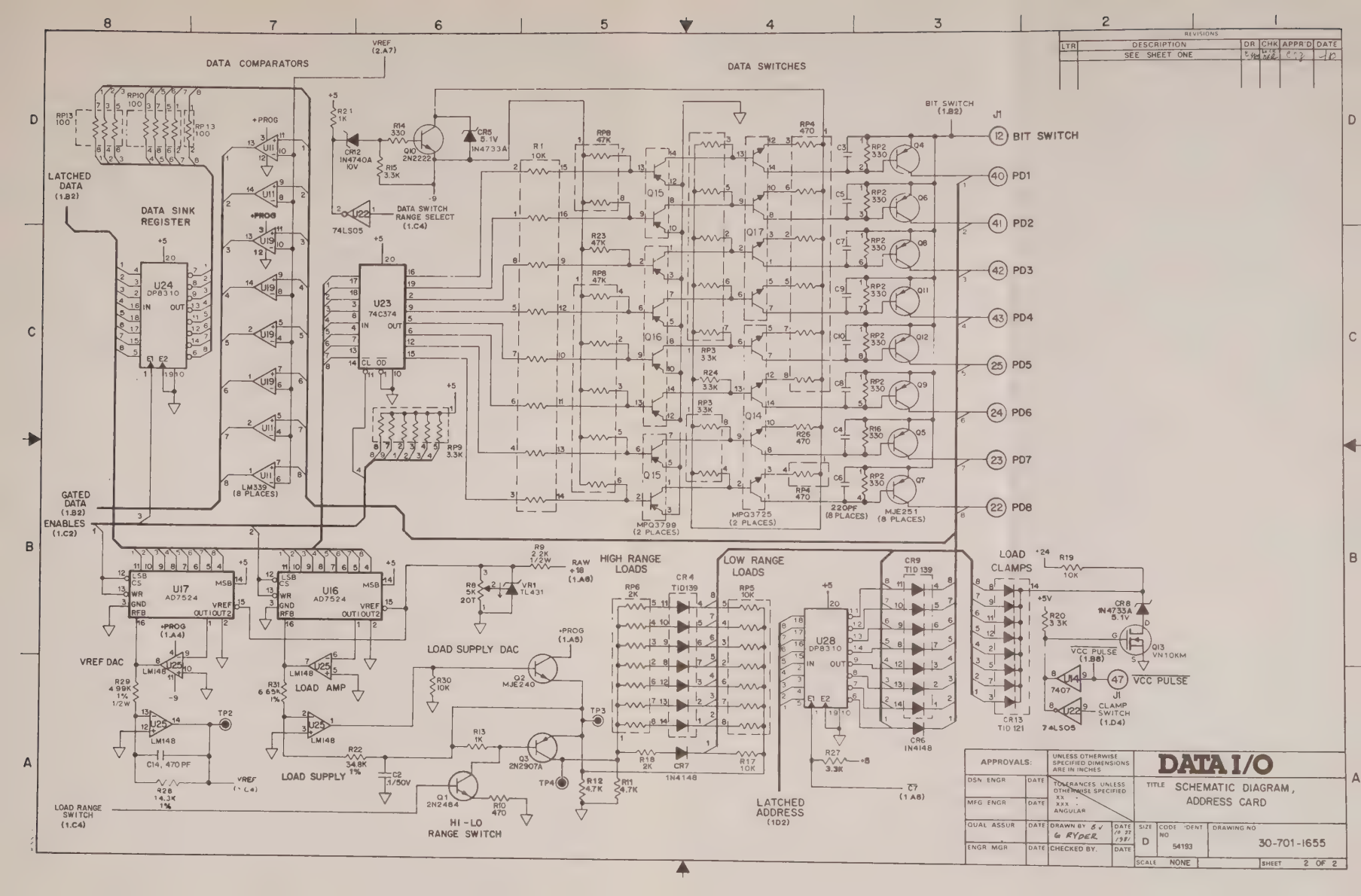
I.C. NO.	+5V	GND
U17-19	16	8
U16,20	20	10
U5,9-11	14	7

APPROVALS:	UNLESS SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
PROJ ENG.	TOLERANCES DECIMALS ANGULAR	TITLE SCHEMATIC DIAGRAM, WAVEFORM GENERATOR
ENG MGR	DO NOT SCALE DRAWING	
QC	DRAWN BY 12-81 JAEHEE KIM	SIZE D CODE IDENT NO 54193 DRAWING NO 30-701-1690
DATE	CHECKED BY:	SCALE 12/2/81 SHEET 1OF 2


REVISIONS
SEE SHEET ONE
J1
VCC
VCC SENSE
CE SUPPLY
BIT SUPPLY
BIT SWITCH
OVERCURRENT
VCC (1.D3)
VCC SENSE (1.D3)
CE SUPPLY (1.C3)
BIT SUPPLY (1.D3)
CURRENT SOURCE REFERENCE (1.B3)
CURRENT SOURCE KILL (1.A3)
BIT SWITCH (1.C2) (1.B8)
SWITCH CONTROL BUS
-5 SUPPLY OVERCURRENT (1.D3)
BIT SWITCH 4,6 (1.B2)
V REF (1.D6)
DAC REF
V REF (2.C8)
CE SUPPLY (2.D8)
ADDRESS SUPPLY (1.A7)
PIN 18
PA11
PIN 20
PIN 21
+5V
+PROG
-9V
ADDRESS SUPPLY
GND
BIT SWITCH CONTROL
PIN 19
PA12
PULL DOWN CONTROL
DATA I/O
SCHEMATIC DIAGRAM,
WAVEFORM GENERATOR
JAEHEE KIM
30-701-1690
12/2/81

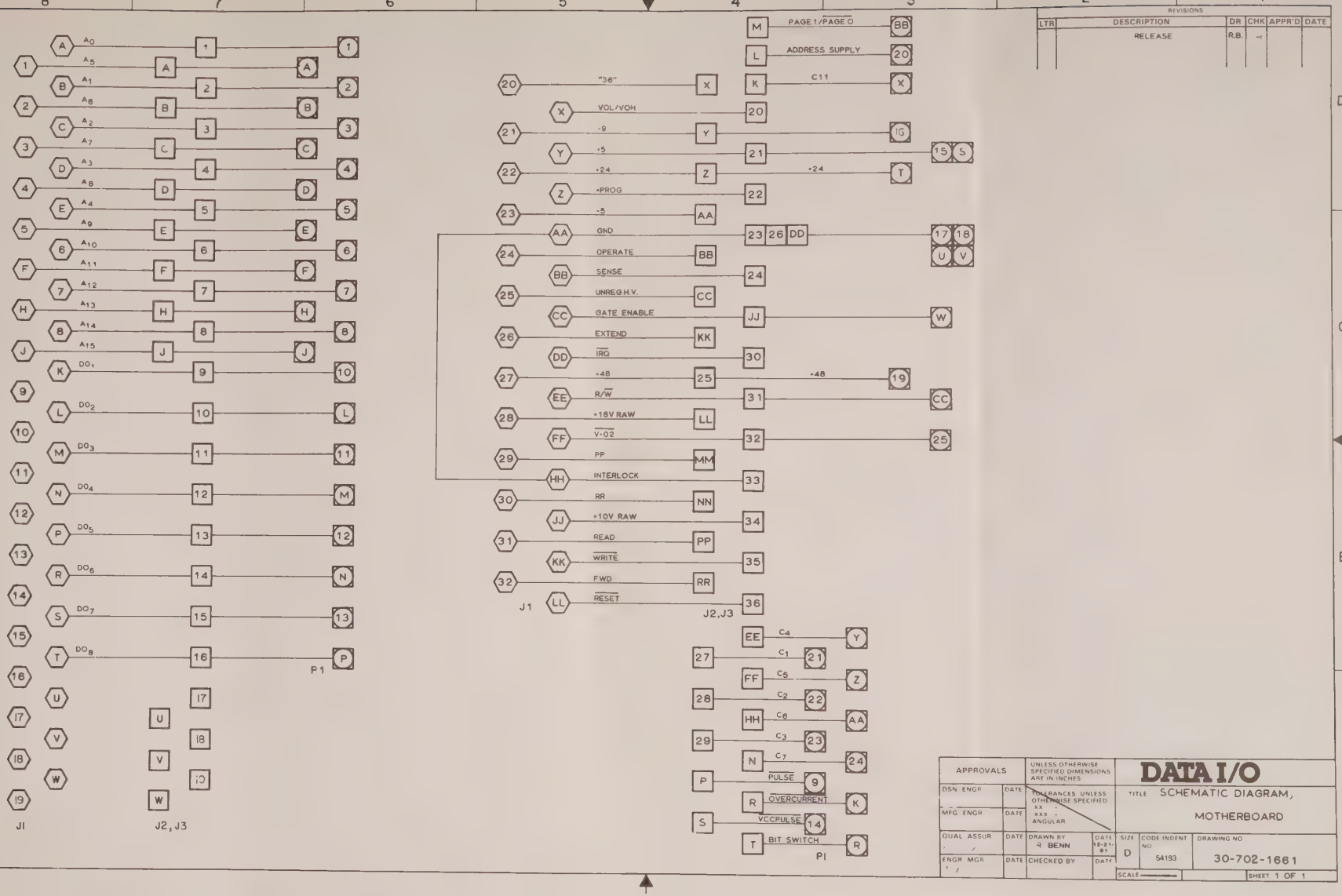


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
A RELEASE BV 9/8
B ECN 4782 CL 2/83
ADDRESS LATCH
L.O. ADDRESS LATCH
H.O. ADDRESS LATCH
SOCKET SELECT LATCH
CURRENT SOURCE LATCH
SECONDARY DECODE
DATA LATCH
COMPARATOR GATE/MUX
SUPPLY COMPARATORS
LATCHED ADDRESS(2.A4)
PIN 18
PIN 19
ADDRESS SUPPLY 5V SELECT
OVER CURRENT
ENABLES(2.B8)
GND
VCC SENSE
PIN 20
BIT SW.(2.D3)
GATED DATA(2.B8)
LATCHED DATA(2.D8)
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 10%.
3 LAST REFERENCE DESIGNATOR USED: TP4, CR13, JP1, J1, C18, U29, Q17, R38, RP13, P1
NOT USED C1, CR11, U5, U7, U8, U9, U10, U12, U13, U15, R25, CR10
4 DELETED AT REV B.
NOT SHOWN
IC. NO. +5 GND
U22 PIN14 PIN7
U14 PIN14 PIN7
UNUSED GATES:
30-701-1655-002 SHOWN
APPROVALS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED XX XXX ANGULAR
DATA I/O
TITLE SCHEMATIC DIAGRAM, ADDRESS CARD
DRAWN BY Barry V.
CHECKED BY
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1655
SCALE NONE
SHEET 1 OF 2
PAGE 1/PAGE 0



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	SEE SHEET ONE	[illegible]	[illegible]	[illegible]	[illegible]

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, ADDRESS CARD	
MFG ENGR	DATE			
QUAL ASSUR	DATE	DRAWN BY G V G RYDER	DATE 10 22 1981	SIZE D
ENGR MGR	DATE	CHECKED BY	DATE	CODE IDENT NO 54193
				DRAWING NO 30-701-1655
			SCALE NONE	SHEET 2 OF 2


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
RELEASE R.B.
J1
J2, J3
P1
J1
J2,J3
P1
PAGE 1/PAGE 0
ADDRESS SUPPLY
C11
"36"
VOL/VOH
-9
-5
+24
+PROG
-5
GND
OPERATE
SENSE
UNREG H.V.
GATE ENABLE
EXTEND
IRQ
+48
R/W
+18V RAW
V-02
PP
INTERLOCK
RR
+10V RAW
READ
WRITE
FWD
RESET
PULSE
OVERCURRENT
VCCPULSE
BIT SWITCH
APPROVALS
DSN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
DRAWN BY R BENN
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM, MOTHERBOARD
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-702-1661
SCALE
SHEET 1 OF 1

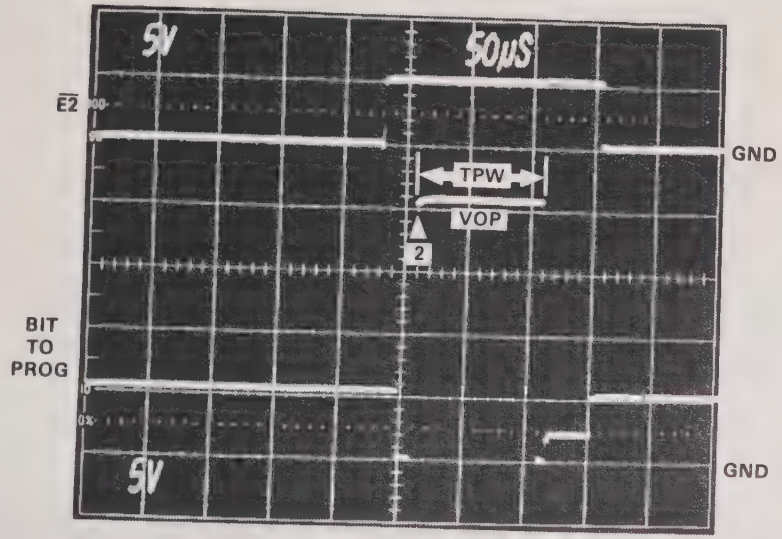
APPENDIX A
ERROR CODES

NOTE

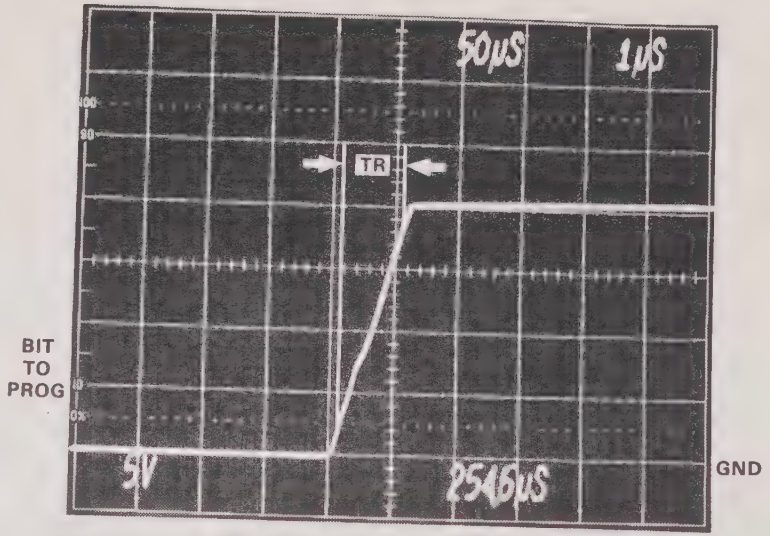
In the case of an error condition, be sure that the family and pinout codes are correct for the PROM installed; refer to table 1-2 in section 1 to cross check family anb pinout codes.

CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
23	First-Pass Verify Error	The device data was incorrect on the first pass of the automatic verify sequence during device programming.
24	Second-Pass Verify Error	The device data was incorrect on the second pass of the automatic verify sequence during device programming.
27	Insufficient RAM	Due to the value of the Begin RAM Address, there is insufficient RAM to program the device, or the total allotment of RAM resident is less than the word limit of the device.
30	No Programming Algorithm	Valid family and pinout codes are not selected, or family code selection not followed by pinout code selection.
31	Excessive Current Drain	The operation aborted due to excessive current drain by a device.
32	Backward Device	The operation aborted due to Vcc level test indicating a backward device.
35	Faulty Chip Select	The operation aborted due to data being present while a device is disabled.
38	Illegal Operation During Calibration	An illegal or invalid operation was attempted during calibration.
37	Socketing Error	Operation aborted due to a low Vcc level indication on sockets presumed to be empty. A device may be in the wrong socket, or two or more devices may be socketed simultaneously.
70	Faulty Bit Supply	The operation aborted due to a faulty bit supply. Do not use UniPak 2™ until repaired.
71	Faulty CS Supply	The operation aborted due to a faulty CS supply. Do not use UniPak 2™ until repaired.
72	Faulty Vcc Supply	The operation aborted due to a faulty Vcc. Do not use UniPak 2™ until repaired.
A1	No Identifier Found	The device does not have an electronic identifier. The electronic identifier mode cannot be used.
A2	Invalid Identifier	The electronic identifier of the device has been read and it indicates that the device cannot be programmed using the selected family and pinout codes. Consult table 1-2 for the correct family and pinout codes. Try again using these codes.
B0	Byte Erase Error	The device does not have a byte erase mode. Block limits must be removed and a chip erase performed. The entire chip may then be reprogrammed.

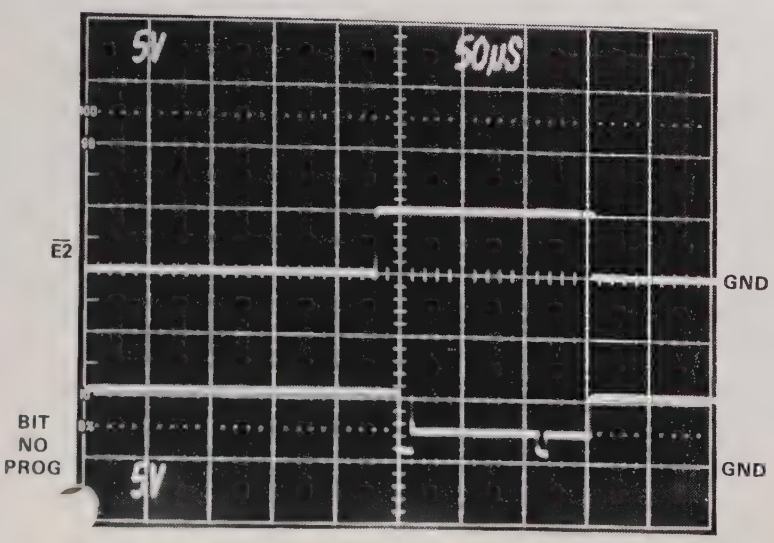
APPENDIX B
TIMING DIAGRAMS

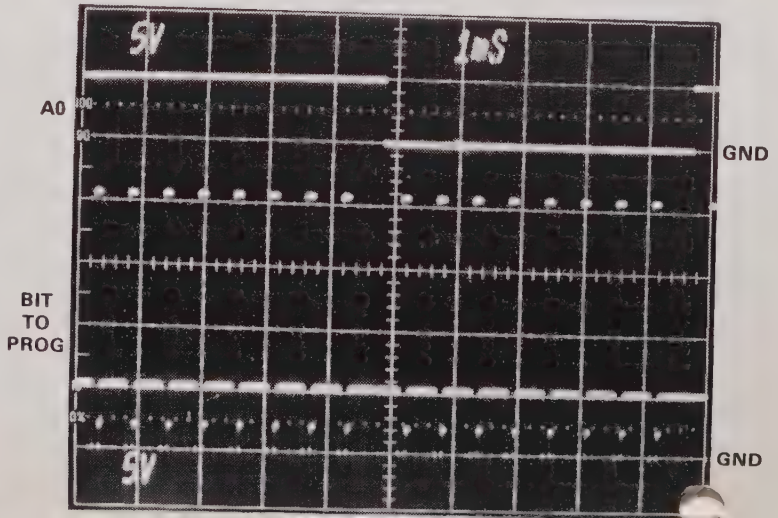


1



2





10-960-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP	20.0	20.5	21.0	V	
	TPW	90	100	110	µs	
	TR	0.5	1.0	3.0	µs	
	TF					NA
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.3	4.4	4.5	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.1	8.1	9.1	V	701-1655/TP4
	Low Load	7.1	8.1	9.1	V	701-1655/TP3
2ND PASS VERIFY	VCC	4.9	5.0	5.1	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.1	8.1	9.1	V	701-1655/TP4
	Low Load	7.1	8.1	9.1	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 01.*
2. *Load RAM with $01 for Family 02.*

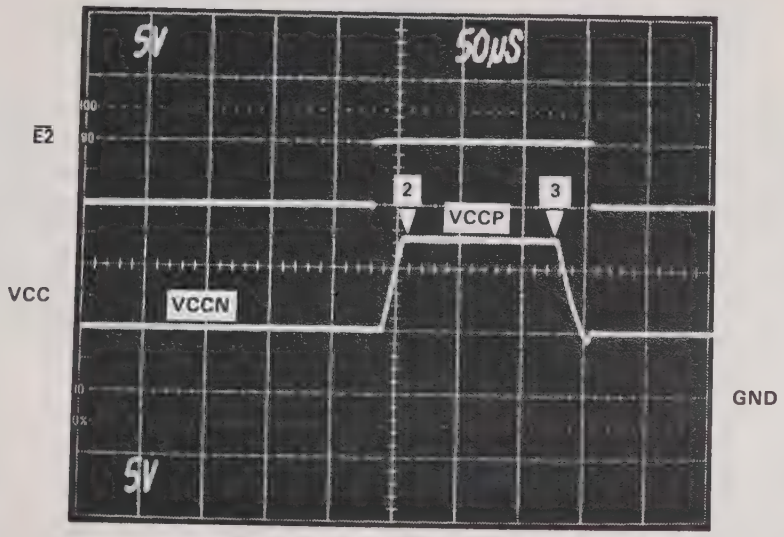
10-950-0059

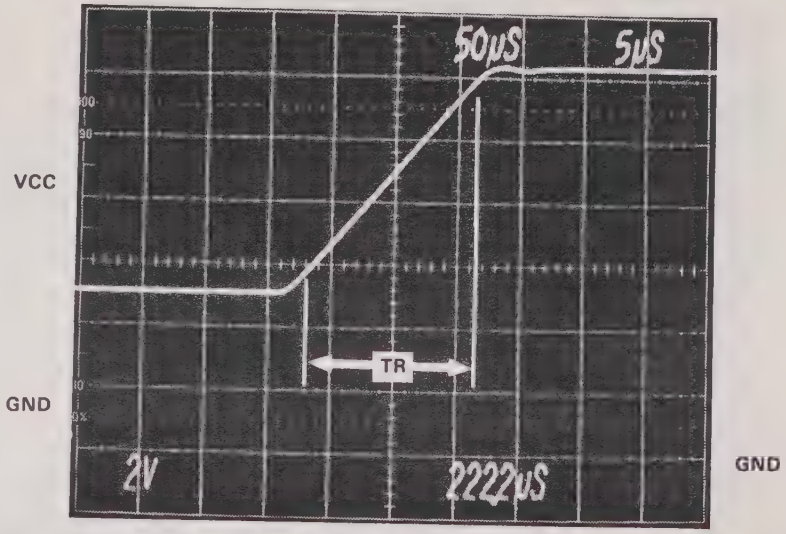
REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJJ	11/82
	C	ECN #4831		KH	5/83

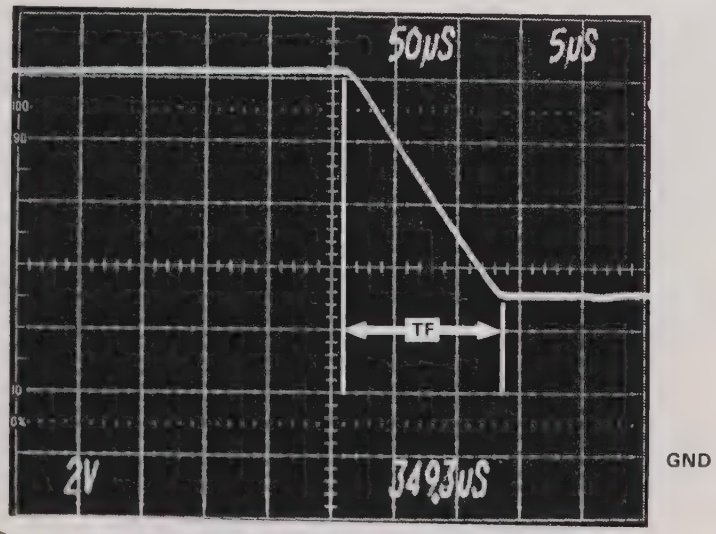
DATA I/O ISSAQUAH, WA

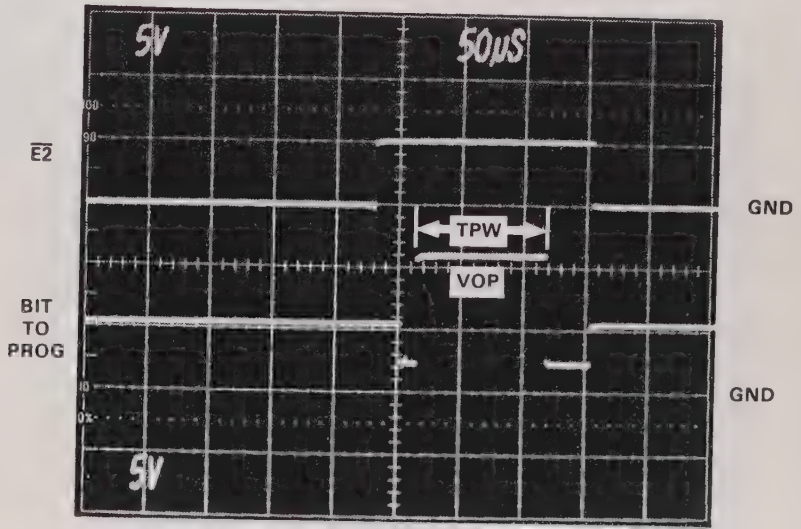
TITLE: TIMING DIAGRAM FAMILY CODES 01, 02		DRAWN BY: PAP CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/1


5V
50µS
E2
2
VCCP
3
VCC
VCCN
GND
5V


50µS
5µS
VCC
GND
TR
2V
2222µS
GND

2


50µS
5µS
VCC
TF
GND
2V
3493µS


5V
50µS
E2
GND
TPW
VOP
BIT
TO
PROG
GND
5V

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12.0	12.0	12.5	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.5	10.5	11.0	V	
	TPW	90	100	110	µs	
	T_R	1.0		25	µs	See note 3
	T_F	1.0		25	µs	See note 3
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	16.3	17.2	18.3	V	701-1655/TP4
	Low Load	16.3	17.2	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.6	1.7	1.8	V	701-1655/TP2
	High Load	12.5	13.5	14.5		701-1655/TP4
	Low Load	12.5	13.5	14.5		701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 05.*
2. *Load RAM with $01 for Family 06.*
3. *Load V_{CC} with a 330Ω ½ watt resistor.*

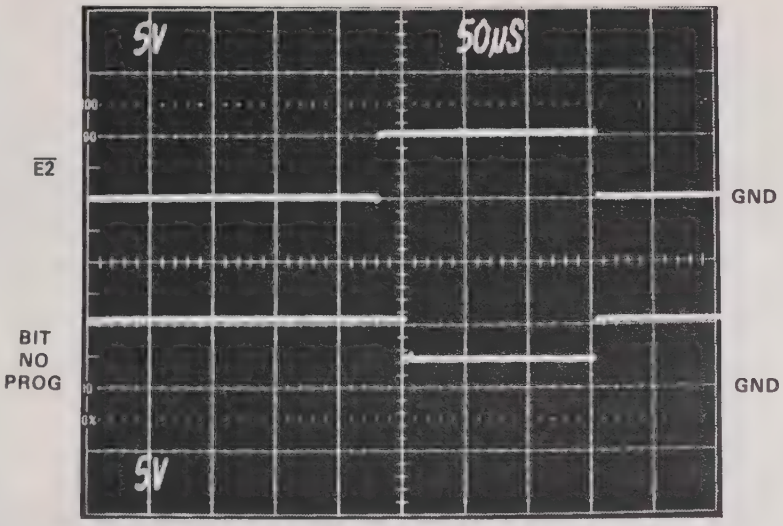
10-950-0059

REVISIONS

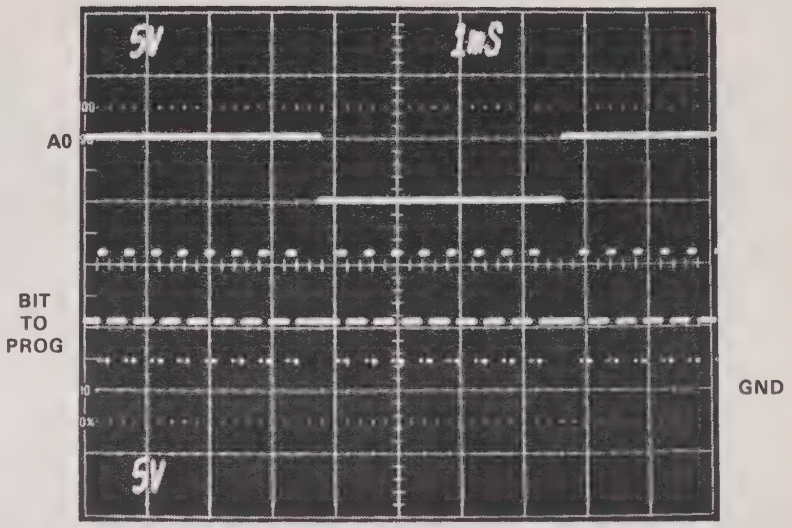
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJZ	11/82
	C	ECN #4831		KH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 05, 06	DRAWN BY:	CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2



5



6

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.T.J.	11/82
	C	ECN #4831		KH	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 05, 06

DRAWN BY:

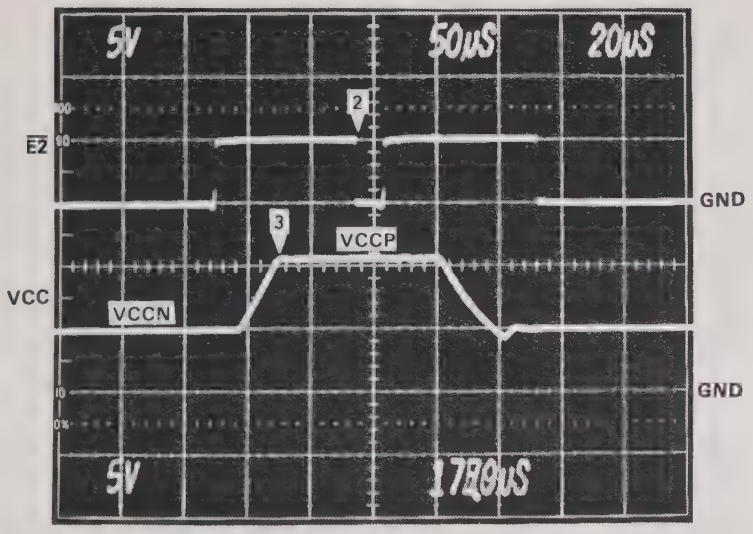
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 2/2

10-950-0059



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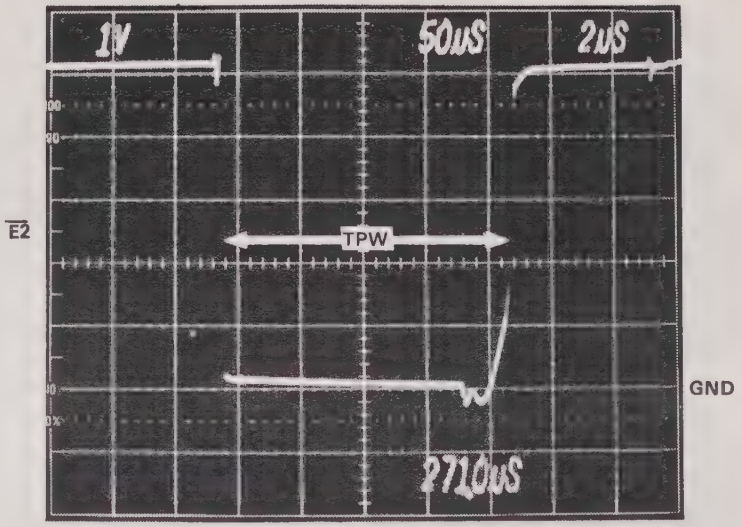

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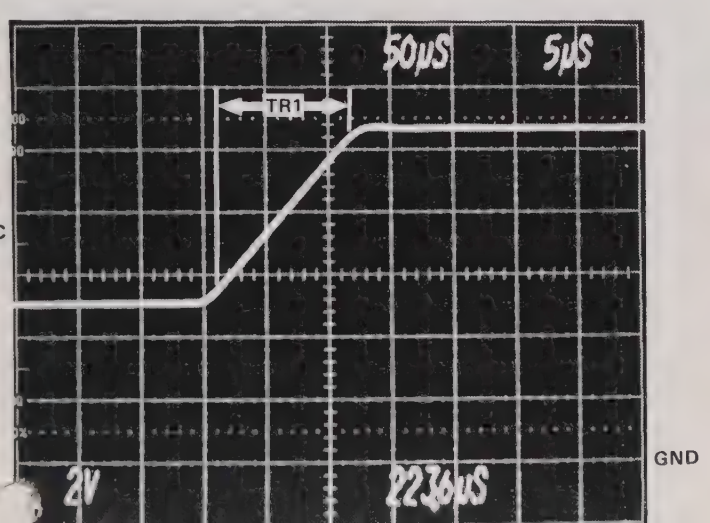
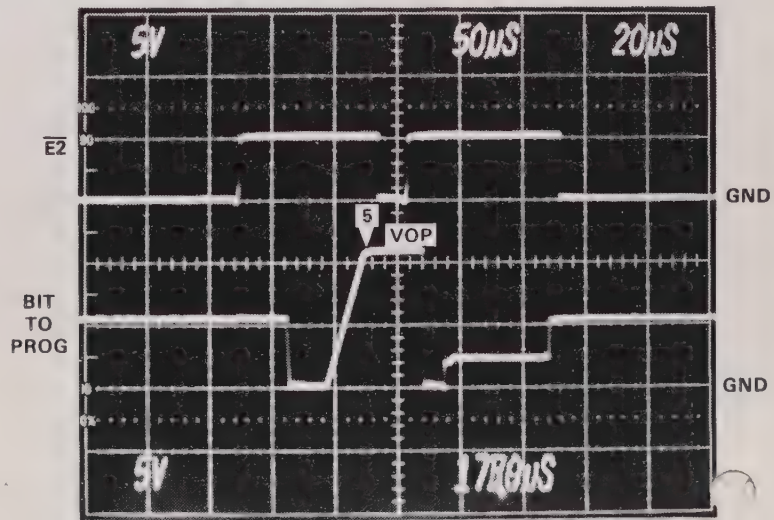




10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	10.0	10.5	11.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.0	10.5	11.0	V	
	TPW	9.0	10.0	11.0	µs	
	TR1	1		25	µs	See note 3
	TR2	1		15	µs	
	TF					NA
	Reject		14		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	3.9	4.0	4.1	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	6.9	7.9	8.9	V	701-1655/TP4
	Low Load	6.9	7.9	8.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	4.9	5.0	5.1	V	
	VREF	1.6	1.7	1.8	V	701-1655/TP2
	High Load	6.0	7.0	8.0	V	701-1655/TP4
	Low Load	6.0	7.0	8.0	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 07.*
2. *Load RAM with $01 for Family 08.*
3. *Loac Vcc with a 330 Ω ½ watt resistor.*

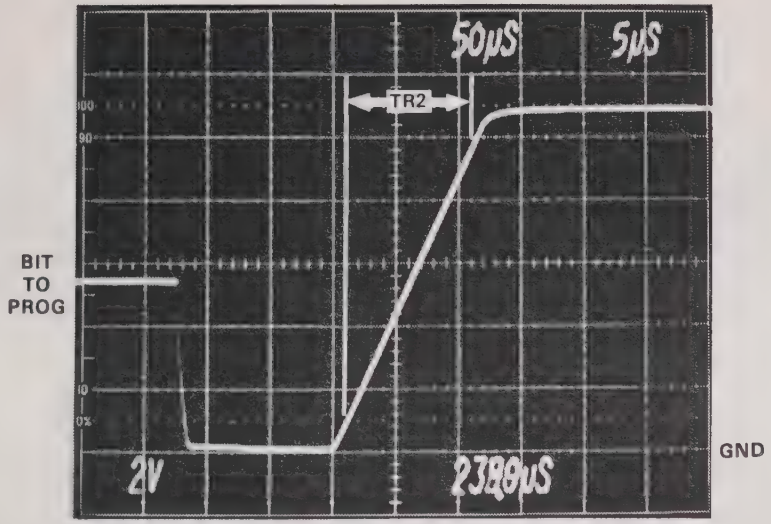
10-950-0059

REVISIONS

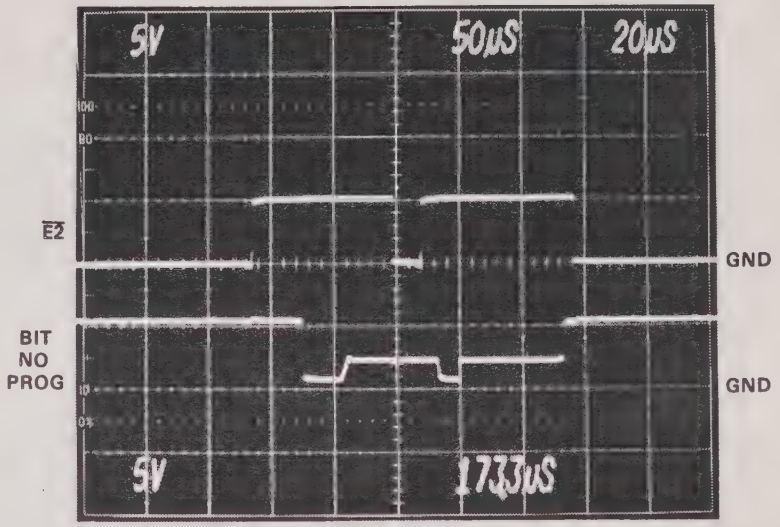
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJZ	11/82
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

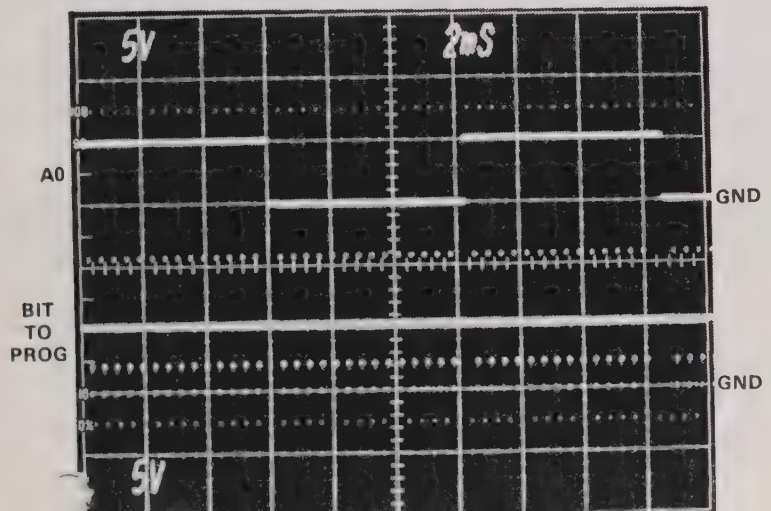
TITLE: TIMING DIAGRAM FAMILY CODES 07, 08	DRAWN BY: ES CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


50µS
5µS
TR2
BIT
TO
PROG
GND
2V
2380µS

5


5V
50µS
20µS
E2
GND
BIT
NO
PROG
GND
5V
1733µS

6


5V
2mS
A0
GND
BIT
TO
PROG
GND
5V

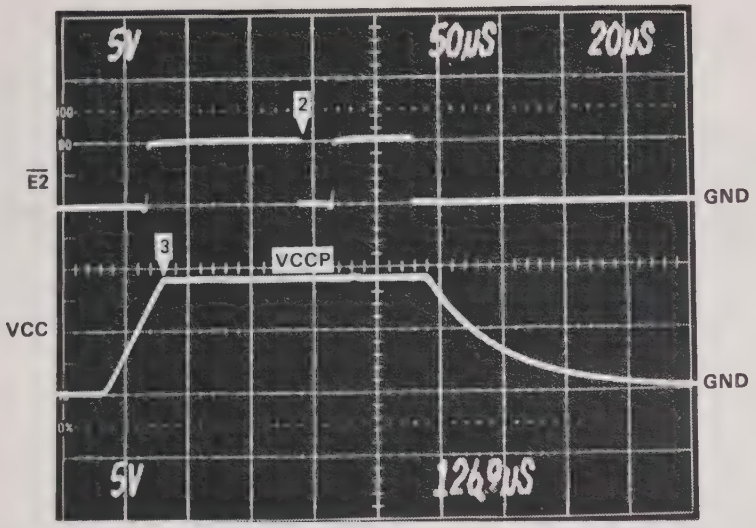
10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.B.J.	11/82
	C	ECN #4831			5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 07, 08	DRAWN BY:	CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2



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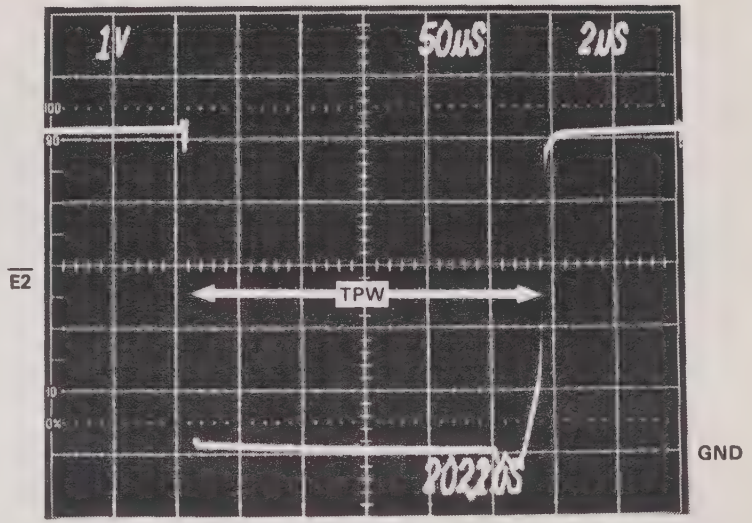

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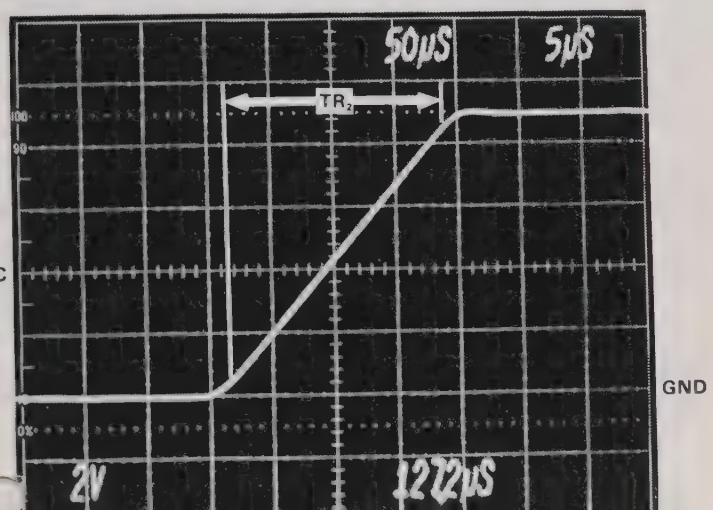
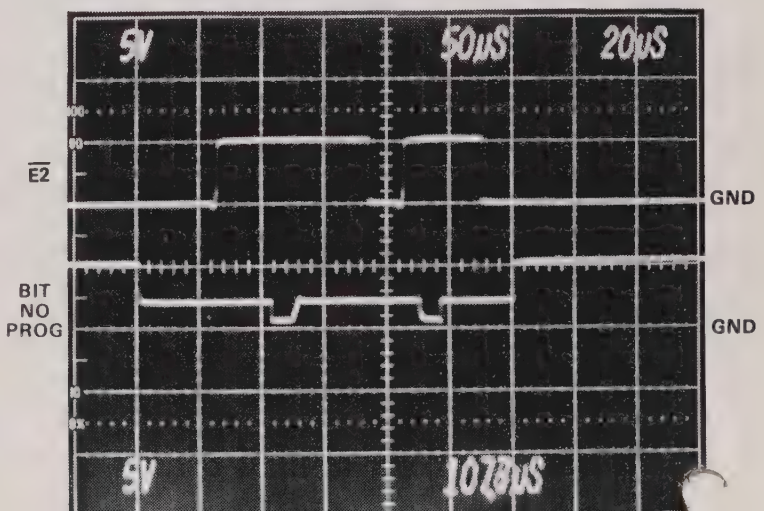




10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	8.5		9.0	V	
	VOP	17.0	17.5	18.0	V	
	TPW	10		15	µs	
	TR1	15		20	µs	
	TR2	5		30	µs	See note 3
	TF	0.2		10	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 09.*
2. *Load RAM with $01 for Family 10.*
3. *Load Vcc with a 330Ω ½ watt resistor.*

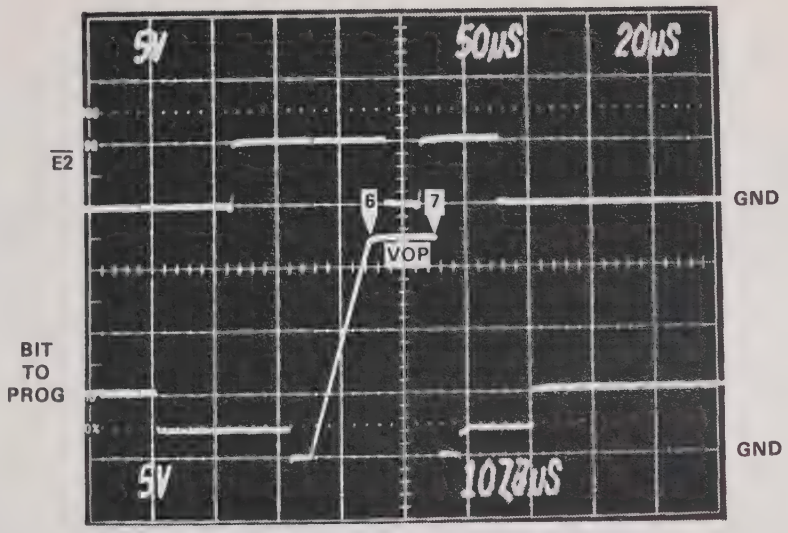
10-950-0059

REVISIONS

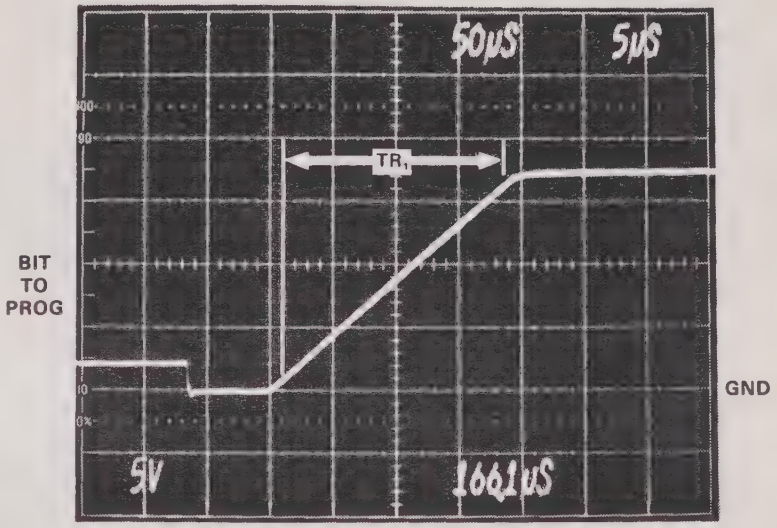
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

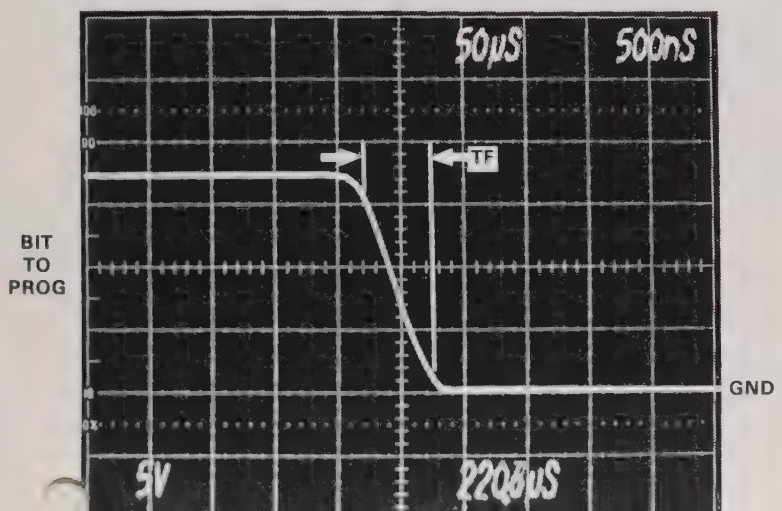
TITLE: TIMING DIAGRAM FAMILY CODES 09, 10		DRAWN BY: ES CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2

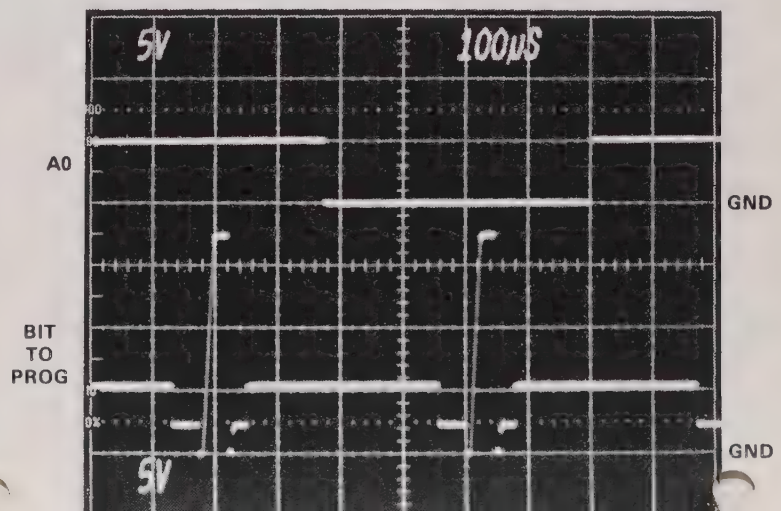

5V
50µS
20µS
E2
6
7
VOP
GND
BIT
TO
PROG
GND
5V
1077µS

5


50µS
5µS
TR1
BIT
TO
PROG
GND
5V
1661µS

6


50µS
500nS
TF
BIT
TO
PROG
GND
5V
2206µS


5V
100µS
A0
GND
BIT
TO
PROG
GND
5V

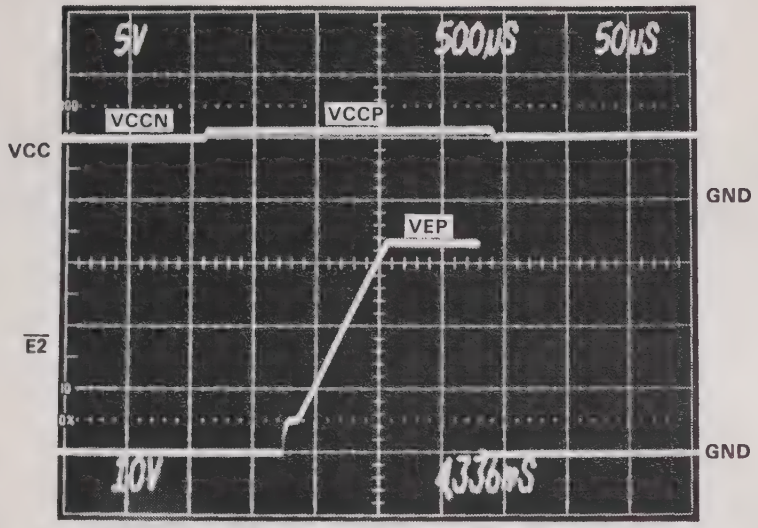
REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		ZH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 09, 10		DRAWN BY: ES CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

10-950-0059



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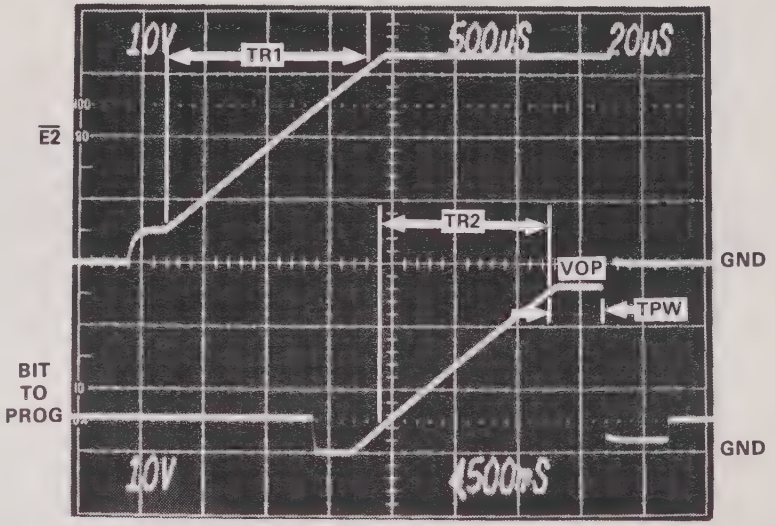

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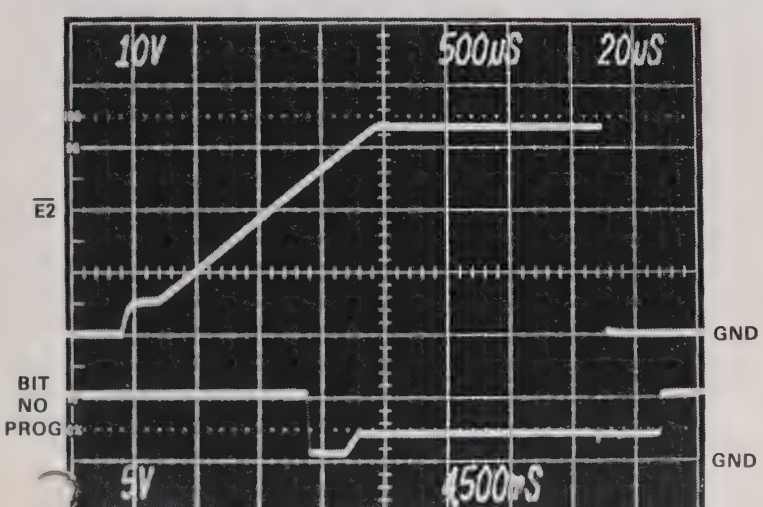
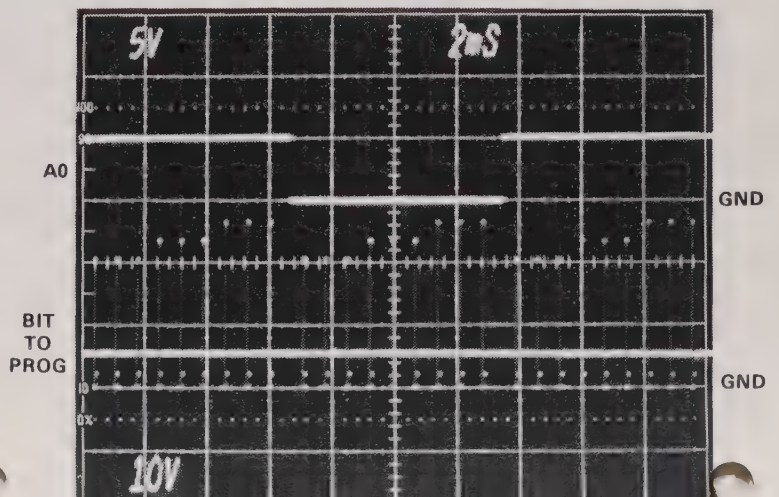




10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.4	5.5	5.6	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	VEP	26	27	28	V	Pulses 1-3
		29	30	31	V	Pulses 4-6
		32	33	34	V	Pulses 7-9
	TPW	10		40	µs	see Note 3
	TR1	53	66	88	µs	see Note 4
	TR2	42	52	69	µs	see Note 4
	TF					NA
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	17.9	18.9	19.9	V	701-1655/TP4
	Low Load	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.6	6.6	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 11.*
2. *Load RAM with $01 for Family 12.*
3. *This is measured at the 90% level of the pulse, and all three pulse levels must meet this specification.*
4. *This is measured from 10% to 90% on the tallest pulse.*

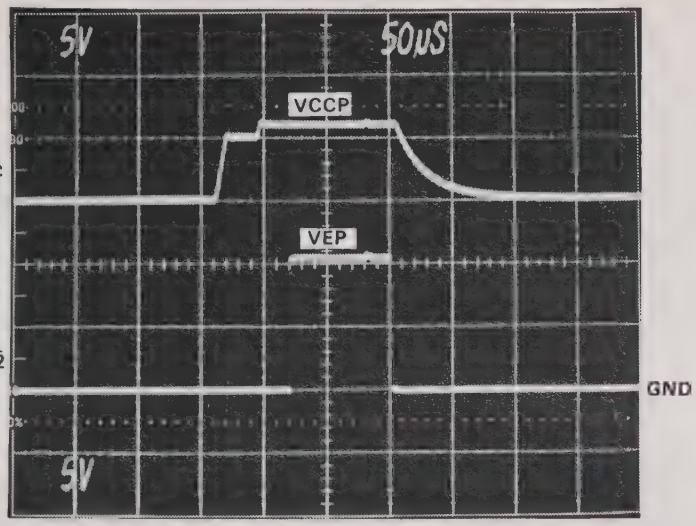
10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		ZH	5/83

DATA I/O ISSAQUAH, WA

TITLE	TIMING DIAGRAM FAMILY CODES 11, 12	DRAWN BY: ES CHECKED BY:	
SIZE	CODE IDENT. NO.	DRAWING NO.	
B	54193	33-950-0059	
SCALE		SHEET 1/1	



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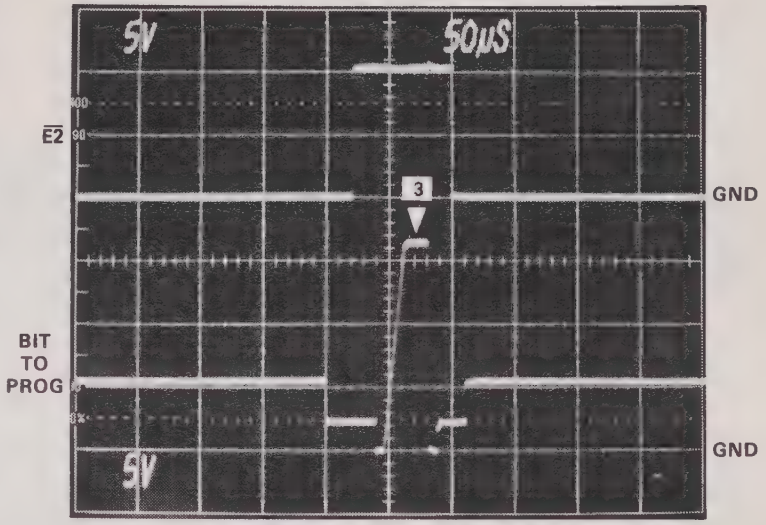

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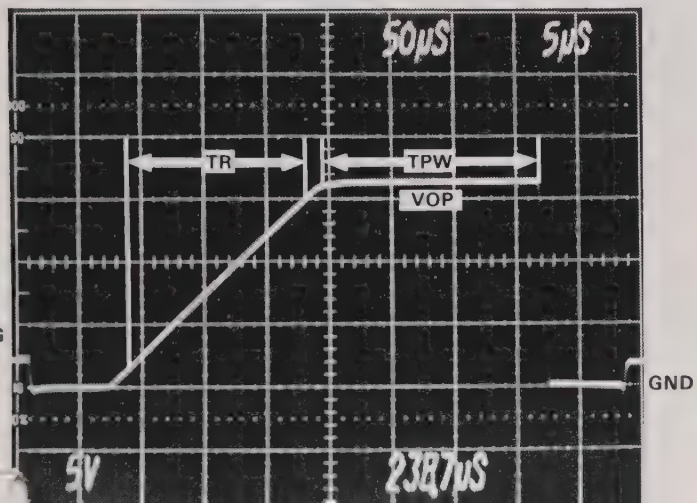
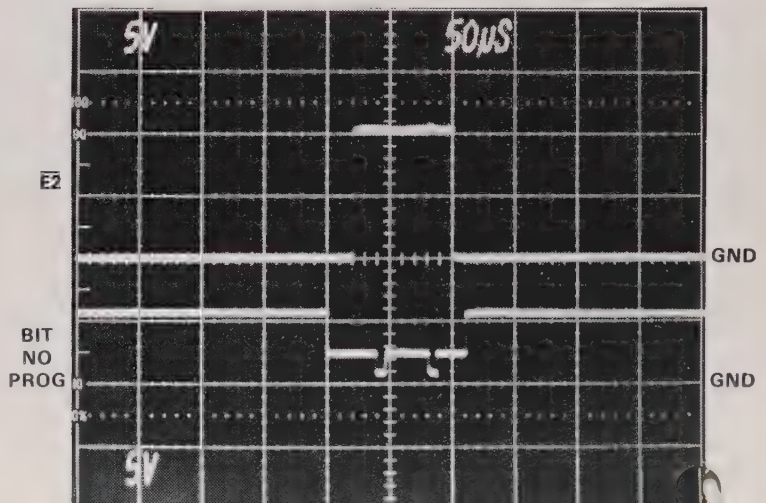




10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP	15.75	16	16.25	V	
	VEP	9.75	10	11.0	V	
	TPW	15		20	µs	
	TR	10	15	20	µs	
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.9	1.0	1.1	V	701-1655/TP2
	High Load	16.3	17.3	18.3	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	12.6	13.6	14.6	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 13.*
2. *Load RAM with $01 for Family 14.*
3. *Photo 6 is for registered devices.*

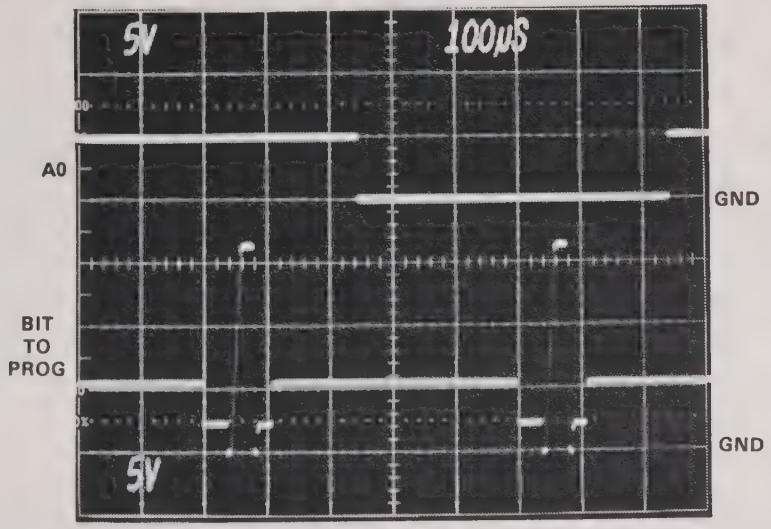
10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z	11/82
	C	ECN #4831		ZF	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM		DRAWN BY:
FAMILY CODES 13, 14		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2



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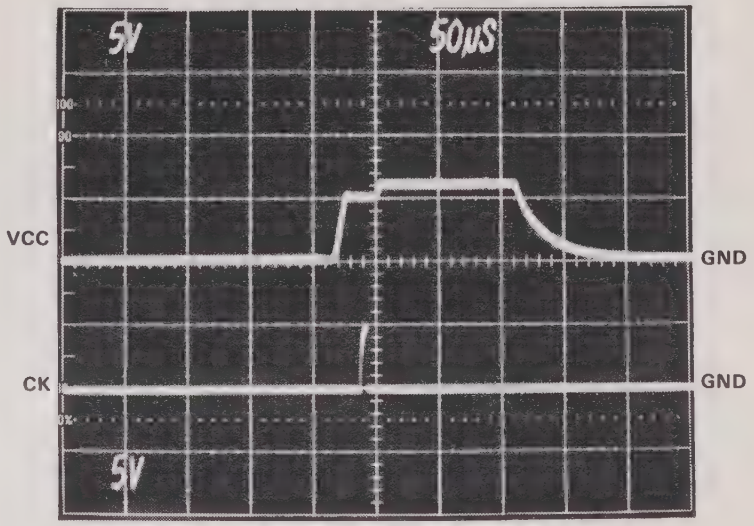


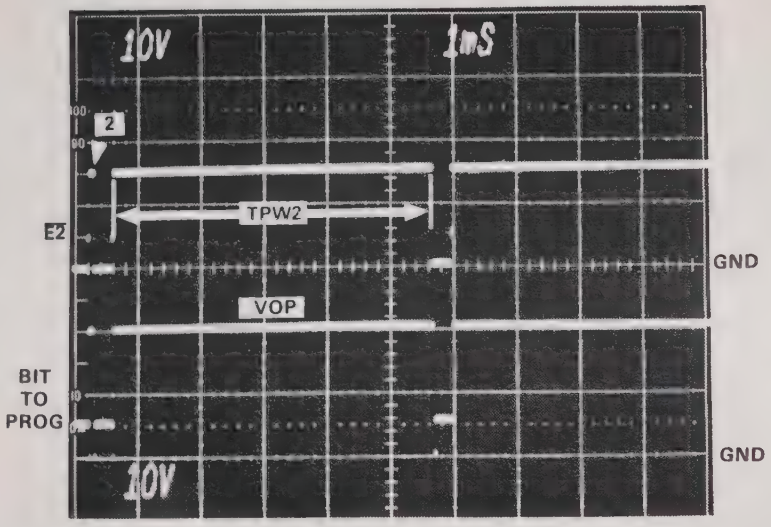
6

10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJJ	11/82
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 13, 14	DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 2/2



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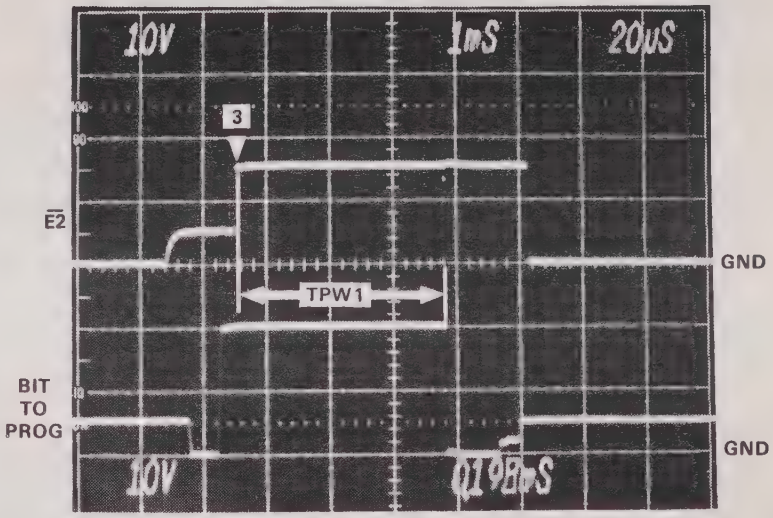

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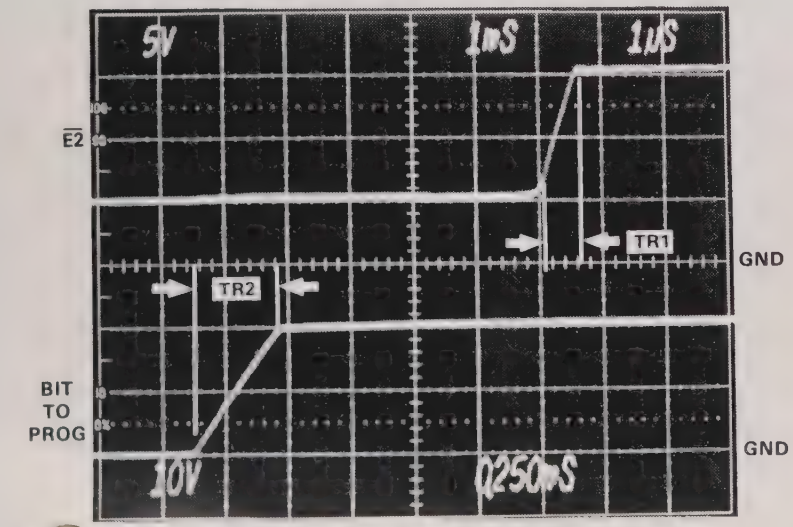

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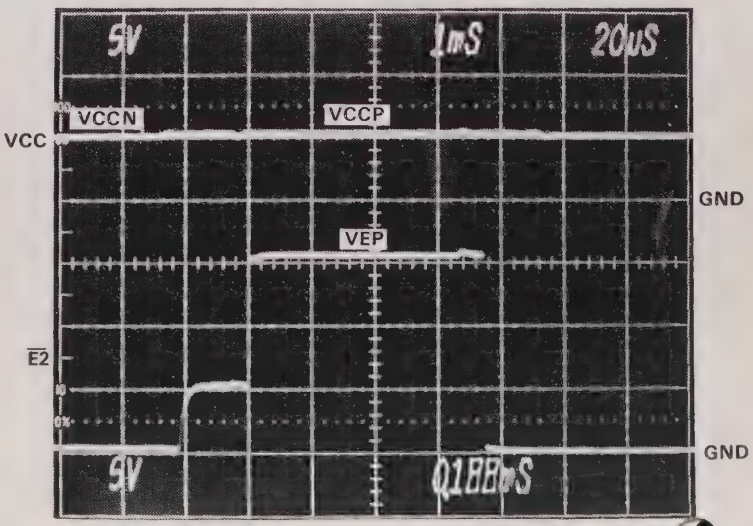


4

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.0	5.25	5.5	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19.5	20.0	20.5	V	
	VEP	14.5	15.0	15.5	V	
	TPW1	50		100	µs	Pulse 1
	TPW2	5		15	ms	Pulses 2-80
	TR1	0.2		0.7	µs	
	TR2	0.6		1.4	µs	
	TF					NA
	Reject		80		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.6	4.7	4.8	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	24.3	25.3	26.3	V	701-1655/TP4
	Low Load	24.3	25.3	26.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	18.0	19.0	20.0	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 15.*
2. *Load RAM with $01 for Family 16.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.B.	11/82
	B	ECN #4772		XX	1/83
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 15, 16

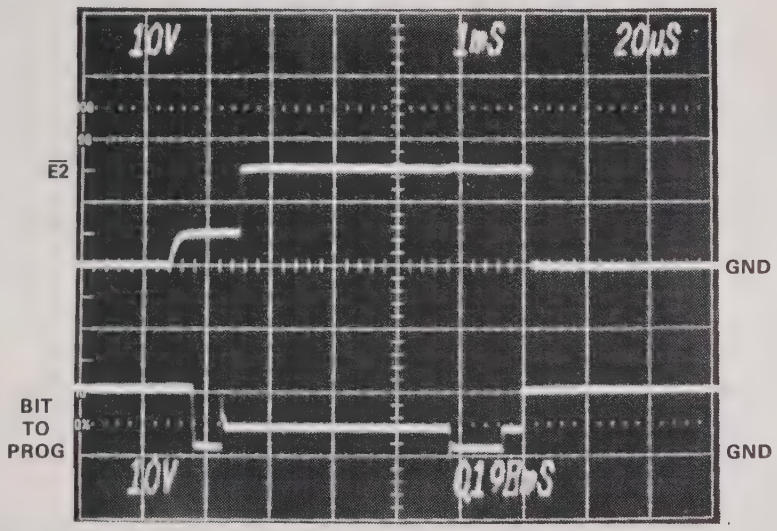
DRAWN BY: EE

CHECKED BY:

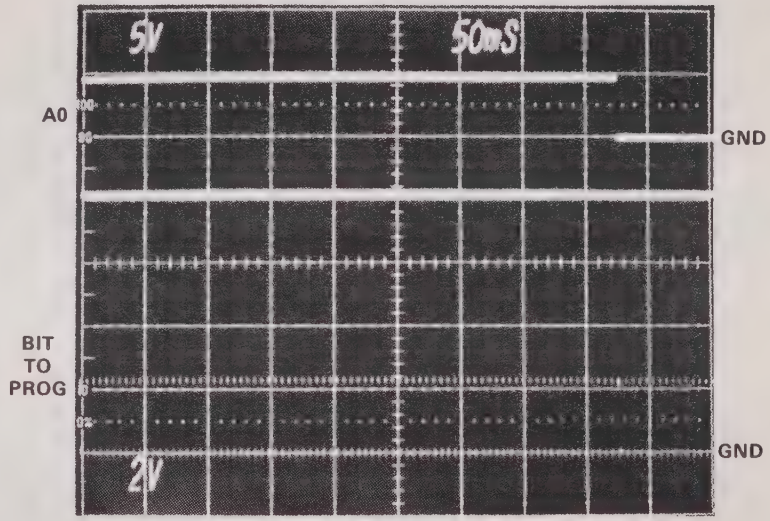
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


10V
1mS
20uS
E2
GND
BIT
TO
PROG
GND
10V
Q19BuS

5


5V
50mS
A0
GND
BIT
TO
PROG
GND
2V

6

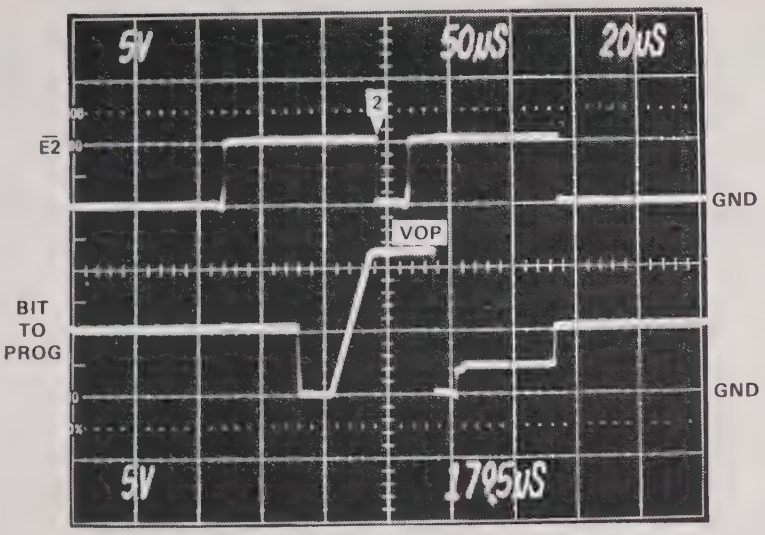
REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		KH	5/83

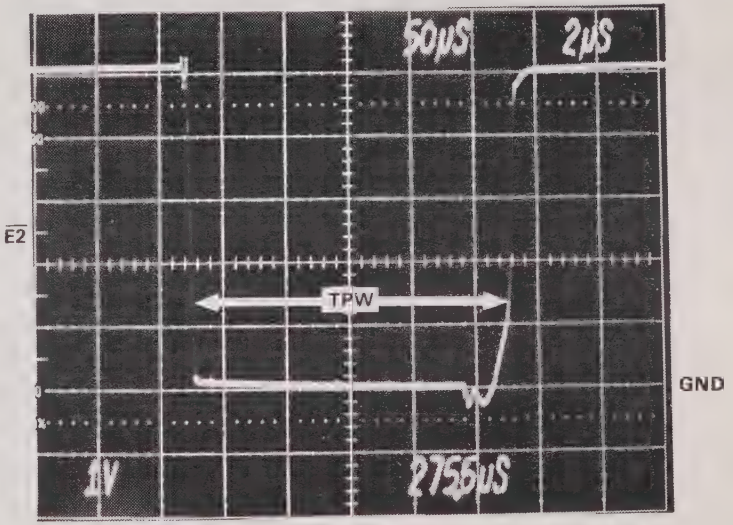
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 15, 16		DRAWN BY: EE CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

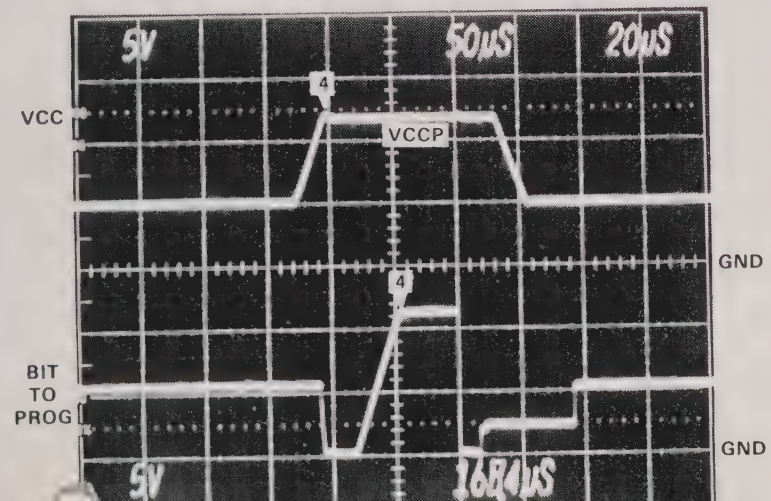
10-950-0059

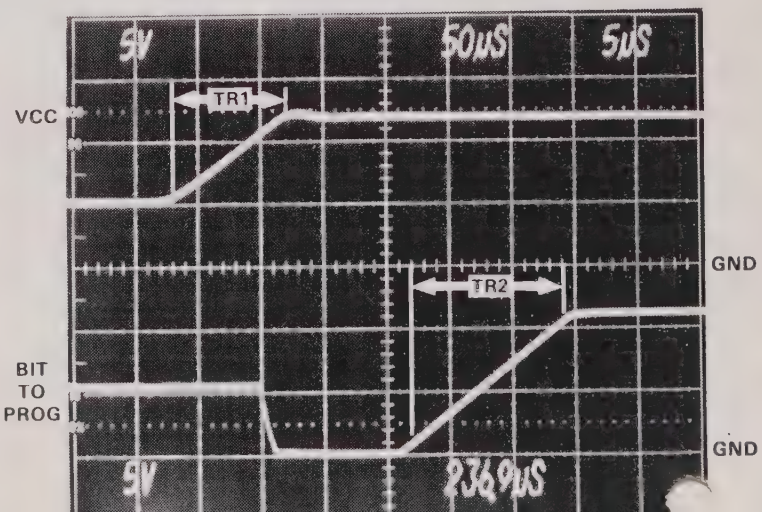


1



2





10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.5	11.7	12.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.5	11.0	11.5	V	
	TPW	9.0	10.0	11.0	µs	
	TR1	1.0		20.0	µs	See note 3
	TR2	1.0		15.0	µs	
	TF					NA
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	4.2	4.3	4.4	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	7.8	8.8	9.8	V	701-1655/TP4
	Low Load	7.8	8.8	9.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 17.*
2. *Load RAM with $01 for Family 18.*
3. *Load Vcc with a 330 Ω ½ watt resistor.*

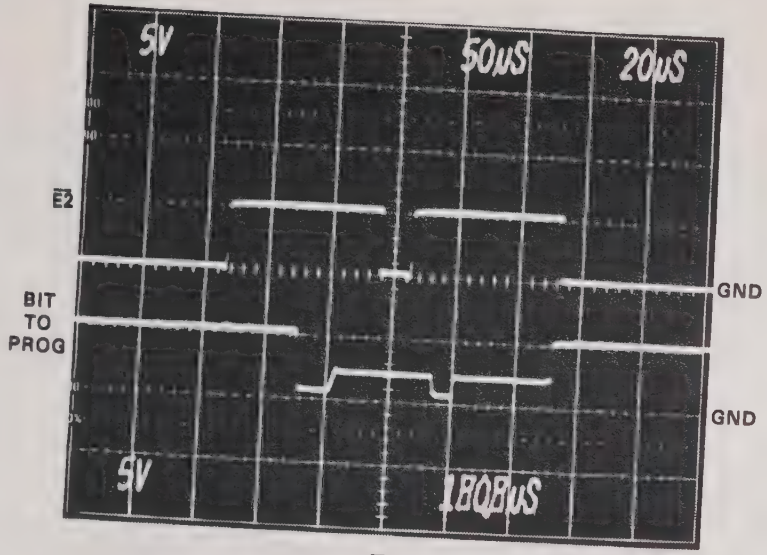
10-950-0059

REVISIONS

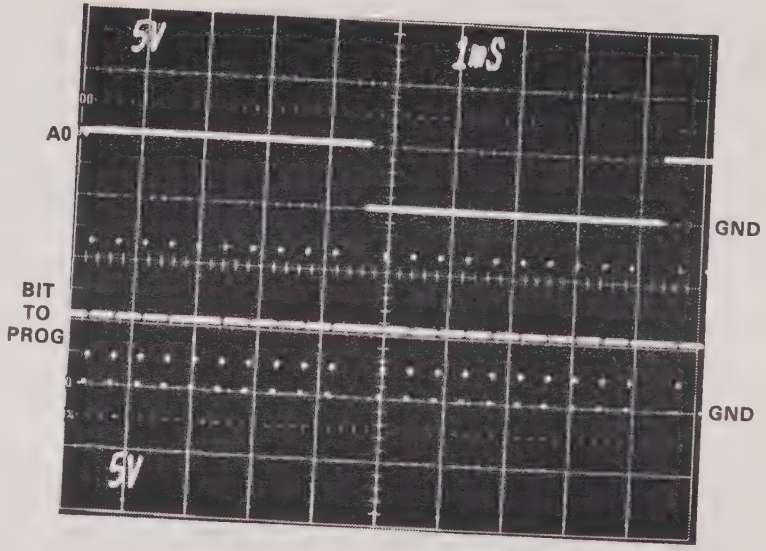
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Relea		C.J.Z.	11/82
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 17, 18	DRAWN BY: EE CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5V
50µS
20µS
E2
BIT
TO
PROG
GND
GND
5V
180µS

5


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

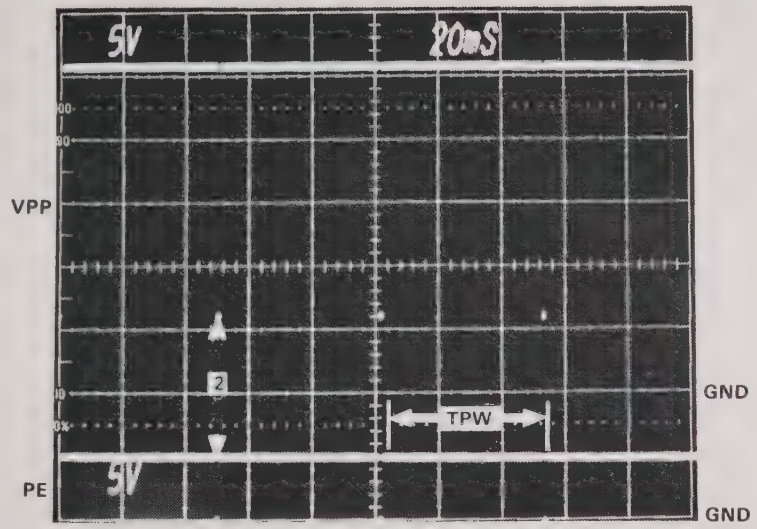
6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.S.3.	11/82
	C	ECN #4831		XX	5/83

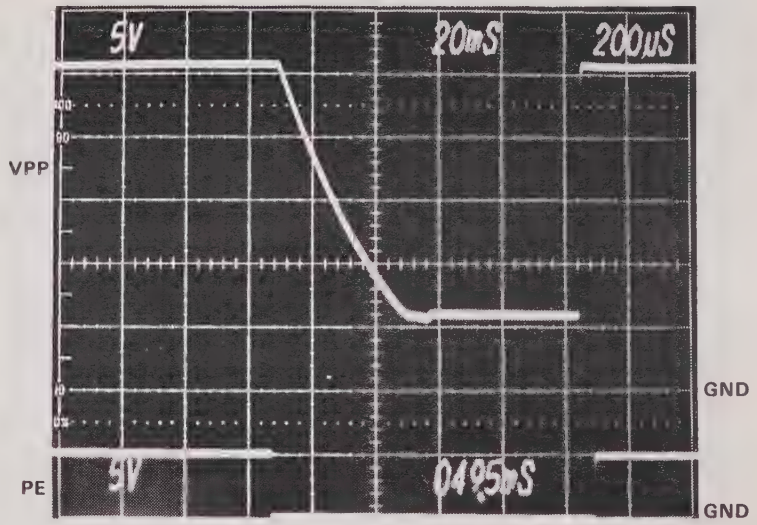
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 17, 18		DRAWN BY: EE CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

10-950-0059



1



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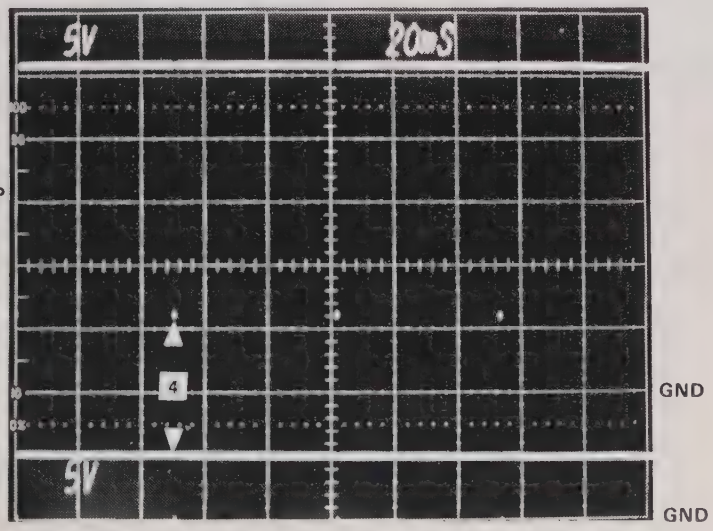

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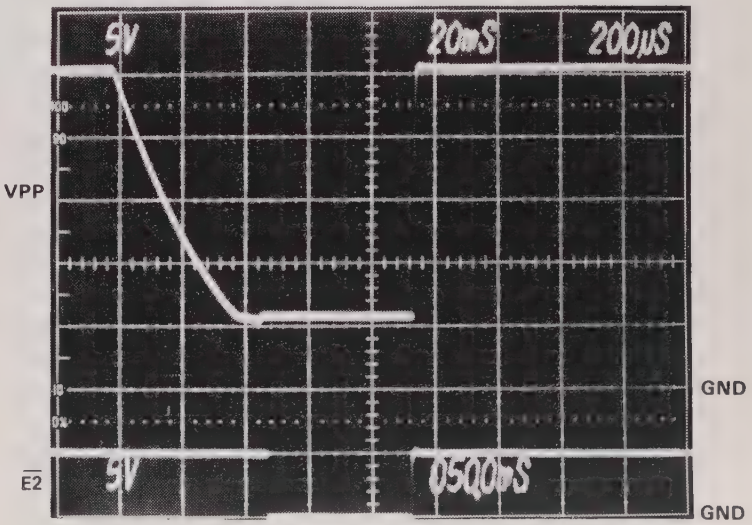

4

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FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	VPPV	0.0	0.0	0.8	V	Pinout 24
	TPW	48	50	52	ms	
	T_R	50			ns	
	T_F	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 19.*
2. *Load RAM with $01 for Family 20, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *Photos 11 and 12 are for Pinout 24.*
4. *Photos 13 and 14 are for Pinout 25.*
5. *Photo 15 is for Pinout 49 using the same set-up as photo 12.*
6. *Photo 16 is for Pinout 50, using the same set-up as photo 14.*

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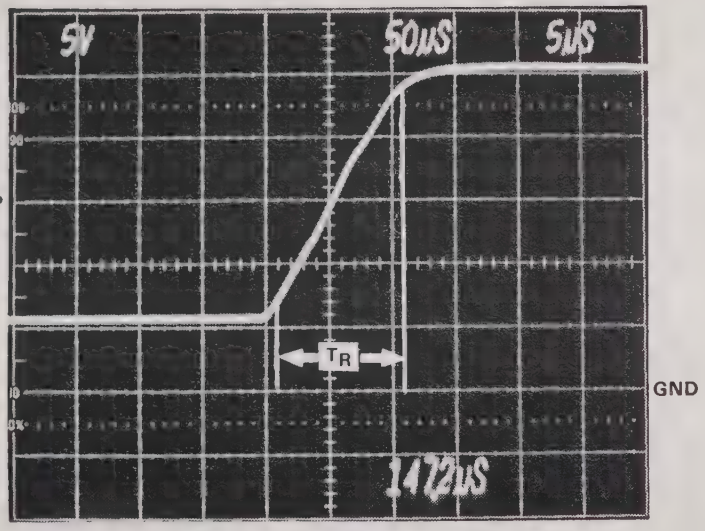
REVISIONS

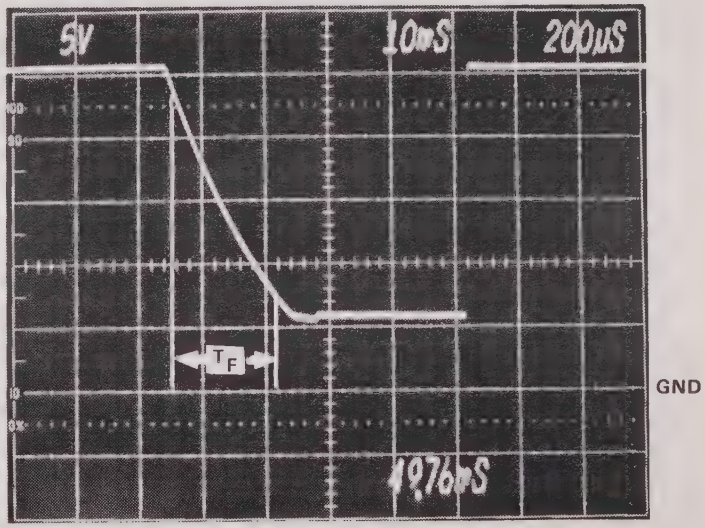
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.JJ.	11/82
	C	ECN #4831		XM	5/83

DATA I/O ISSAQUAH, WA

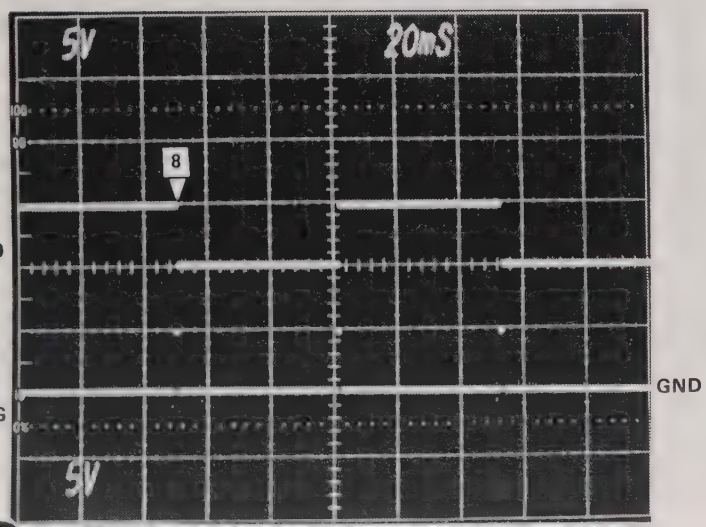
TITLE: TIMING DIAGRAM FAMILY CODES 19, 20	DRAWN BY:	CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/3

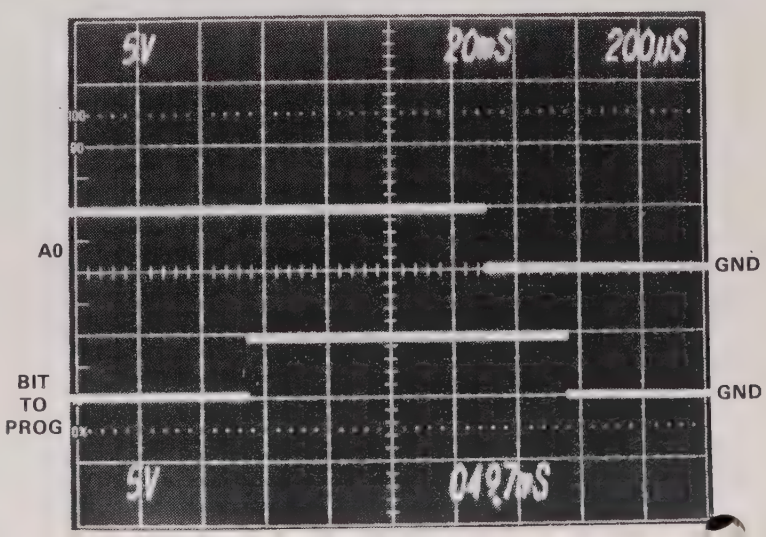

5V
50µS
5µS
VPP
T_R
GND
1.72µS

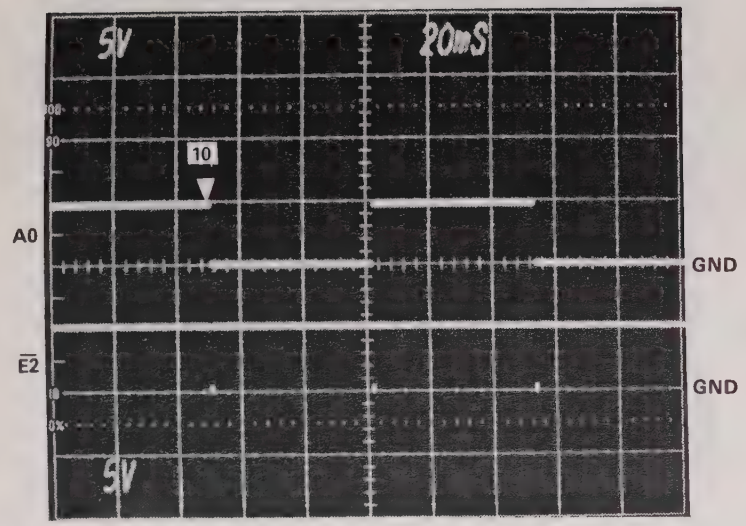
5


5V
10mS
200µS
T_F
GND
4.76mS

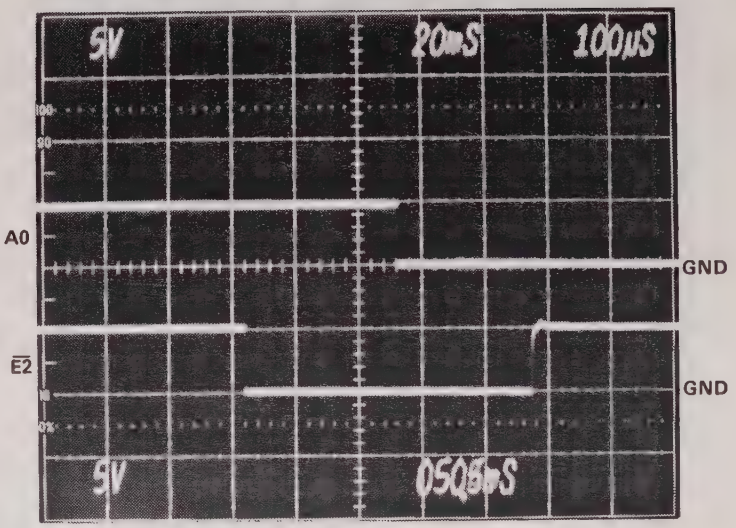
6


5V
20mS
8
A0
BIT
TO
PROG
GND
5V


5V
20mS
200µS
A0
GND
BIT
TO
PROG
GND
5V
4.97mS



9



10

10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.3.	11/82
	C	ECN #4831		TH	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 19, 20

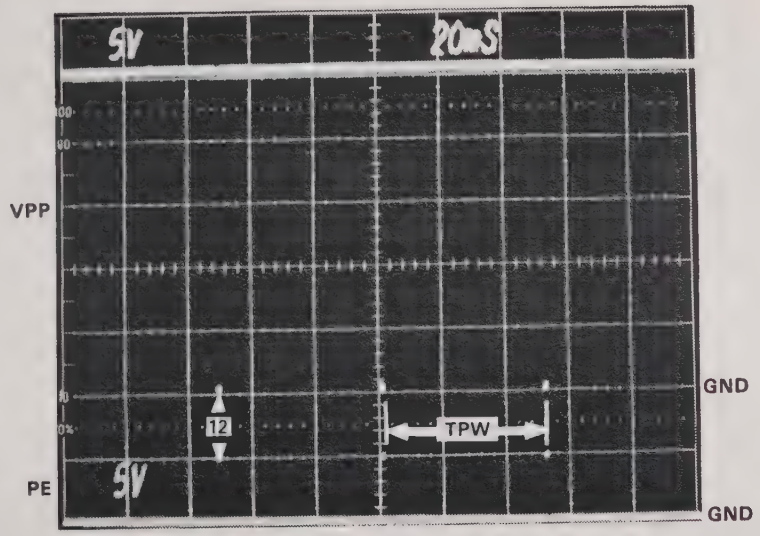
DRAWN BY:

CHECKED BY:

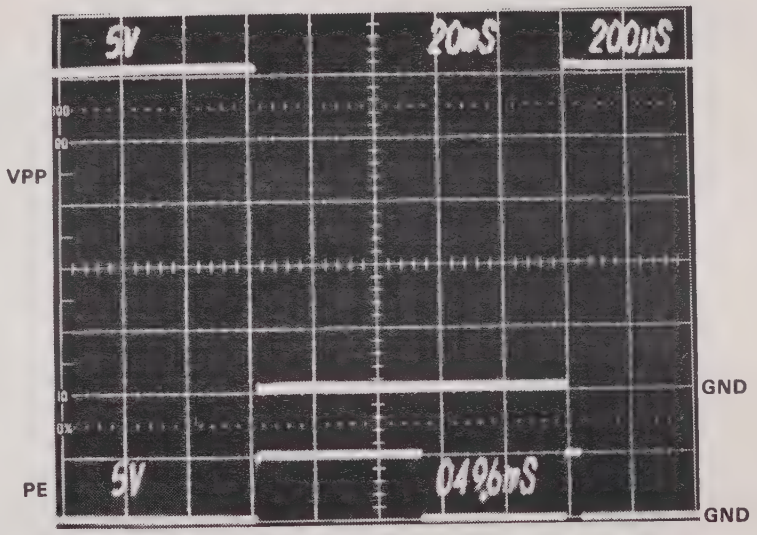
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

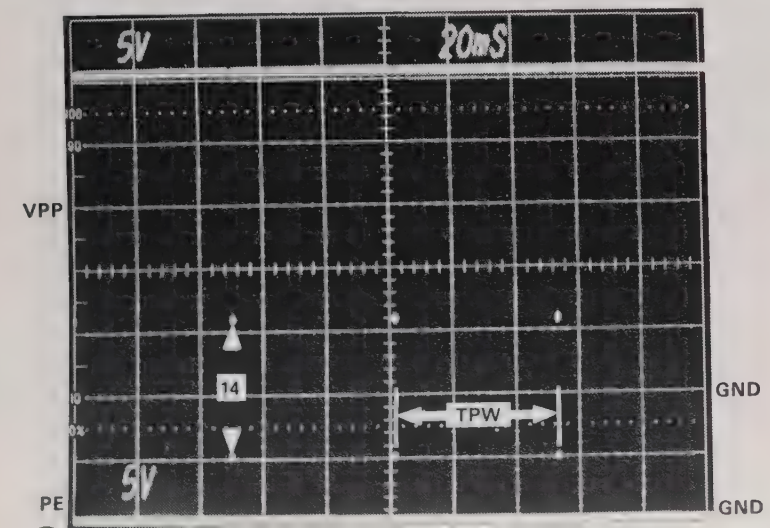
SHEET 2/3

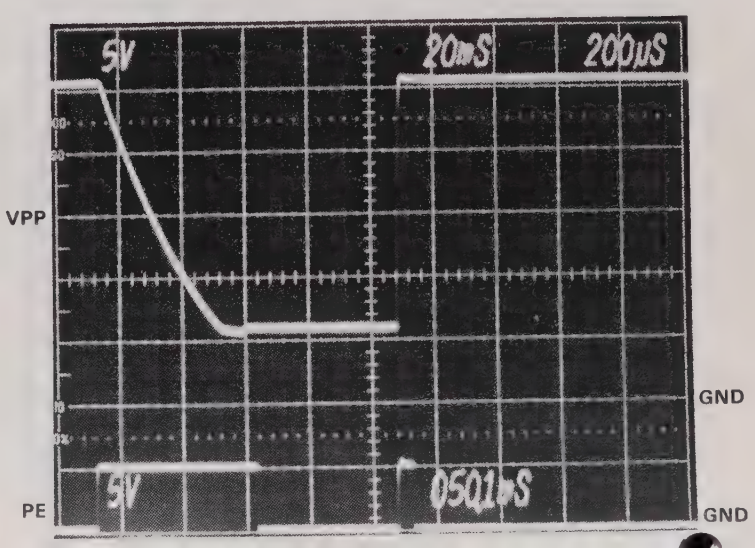


11

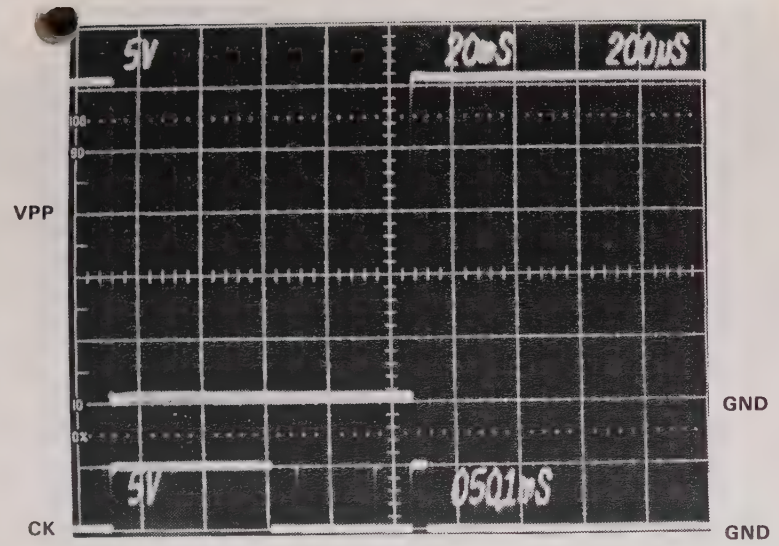


12





10-950-0059



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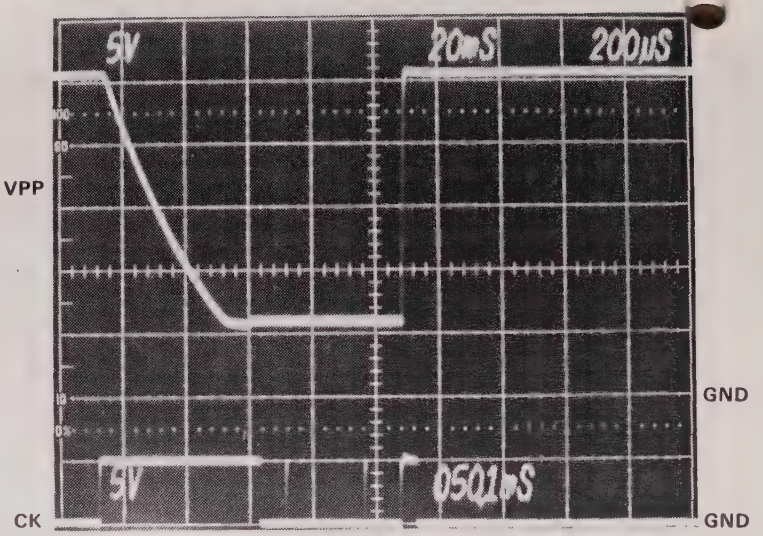

16

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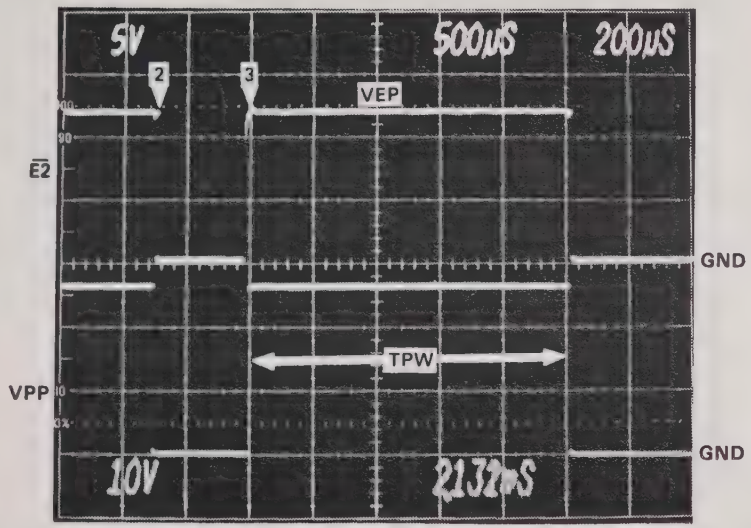
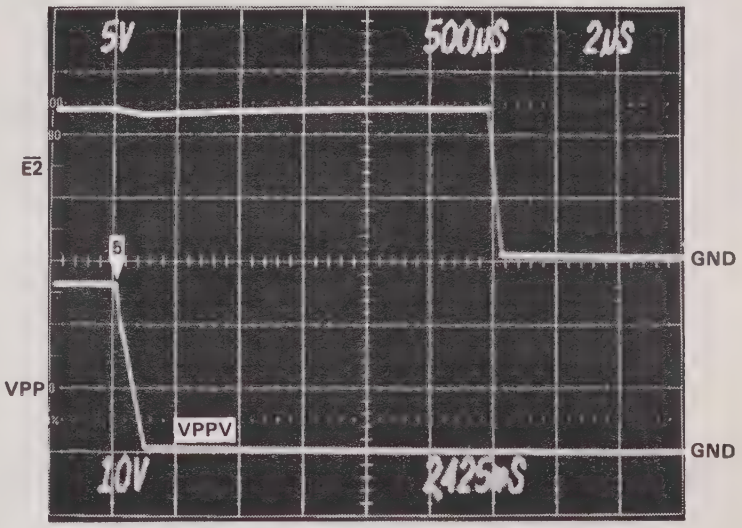
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

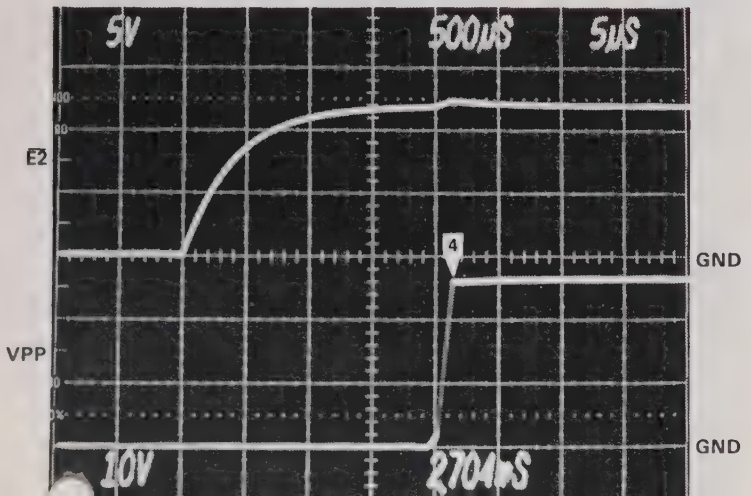
TITLE: TIMING DIAGRAM FAMILY CODES 19, 20		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3/3

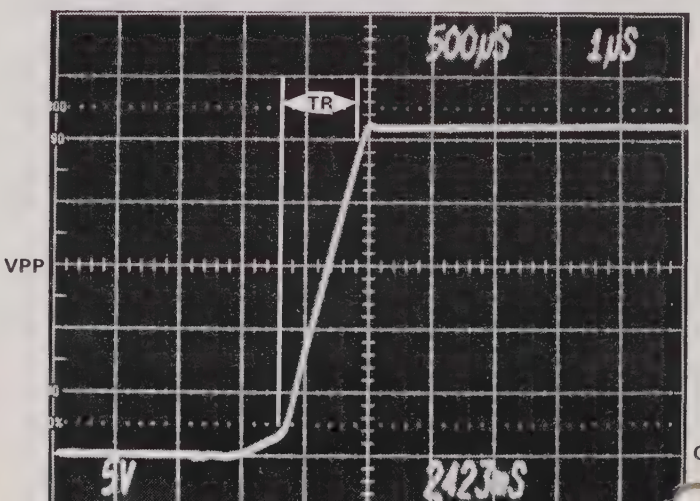

5V
500µS
200µS
2
3
VEP
E2
GND
TPW
VPP
GND
10V
2132mS

1


5V
500µS
2µS
E2
5
GND
VPP
VPPV
GND
10V
2425mS

2


5V
500µS
5µS
E2
4
GND
VPP
GND
10V
2704mS


500µS
1µS
TR
VPP
GND
5V
2423mS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0	0.0	1.0	V	
	VEP	11.4	12.0	12.6	V	
	VBB	-5.25	-5.00	-4.75	V	Not Shown
	VDD	11.4	12.0	12.6	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5	1.0	2.0	µs	
	TF	0.5	1.0	2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 21.*
2. *Load RAM with $01 for Family 22, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address.*

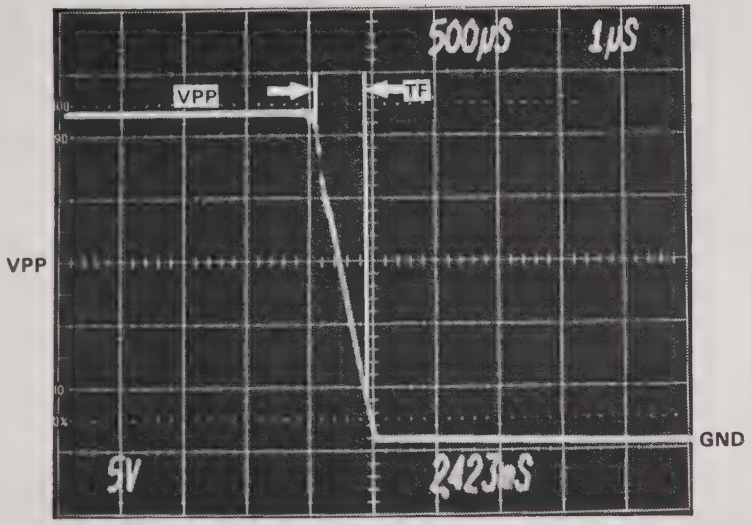
10-960-0059

REVISIONS

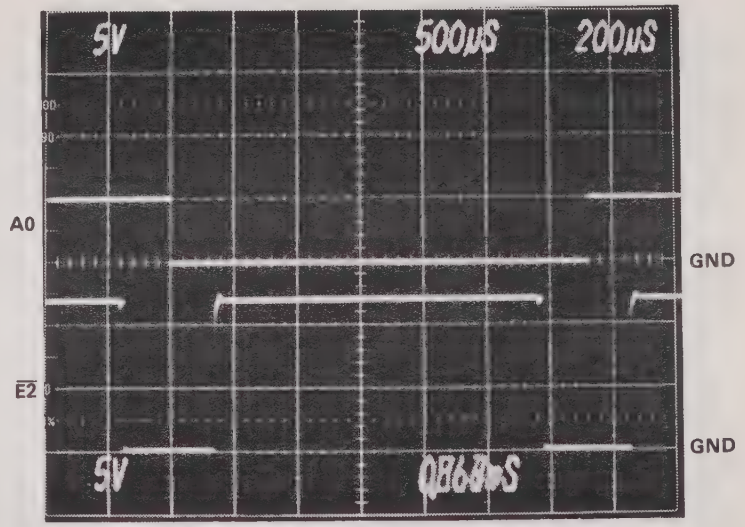
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

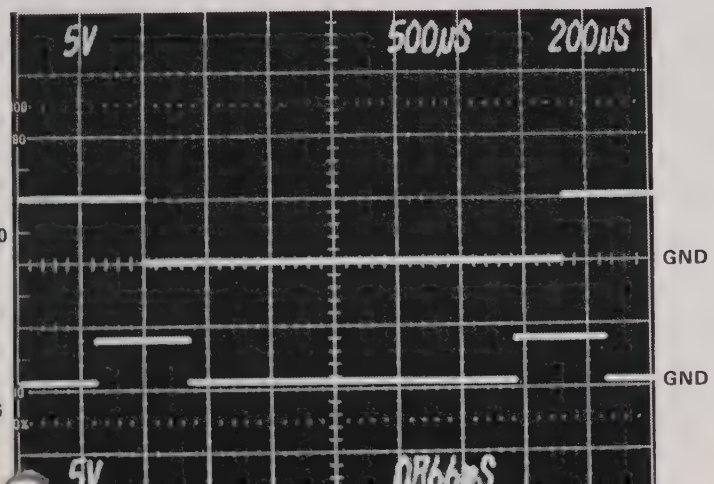
TITLE: TIMING DIAGRAM FAMILY CODES 21, 22	DRAWN BY: EE CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2

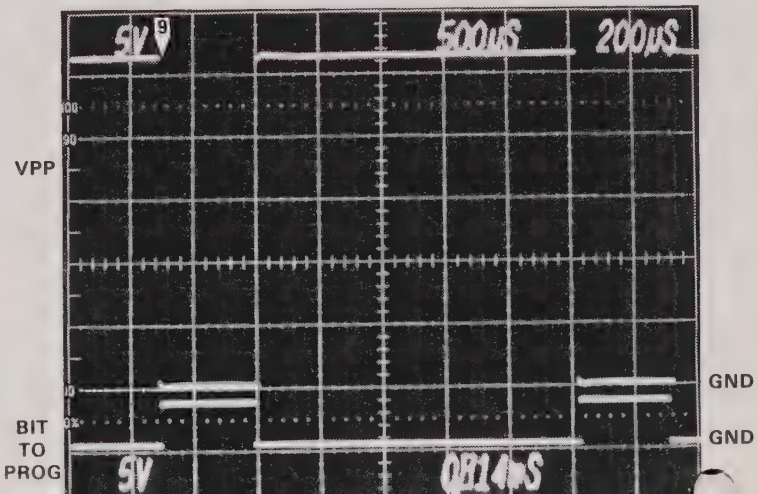


5

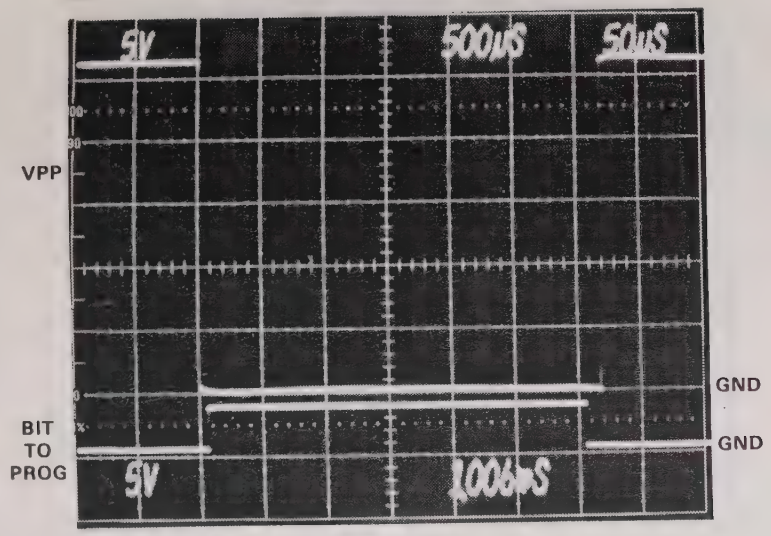


6





10-950-0059



9

10-950-0059

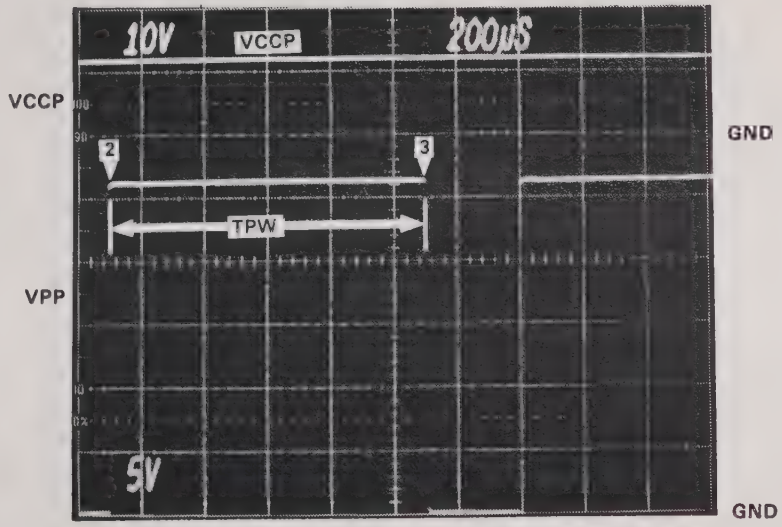
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		XA	5/83

DATA I/O ISSAQUAH, WA

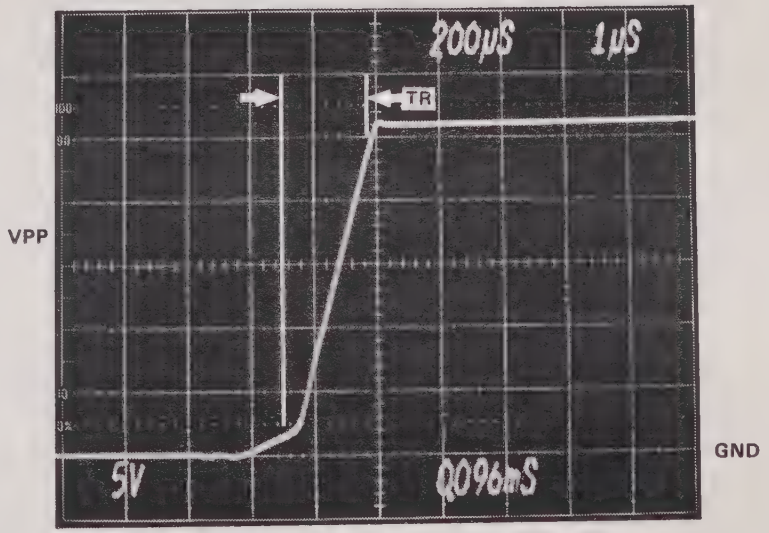
TITLE: TIMING DIAGRAM FAMILY CODES 21, 22	DRAWN BY: ES CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

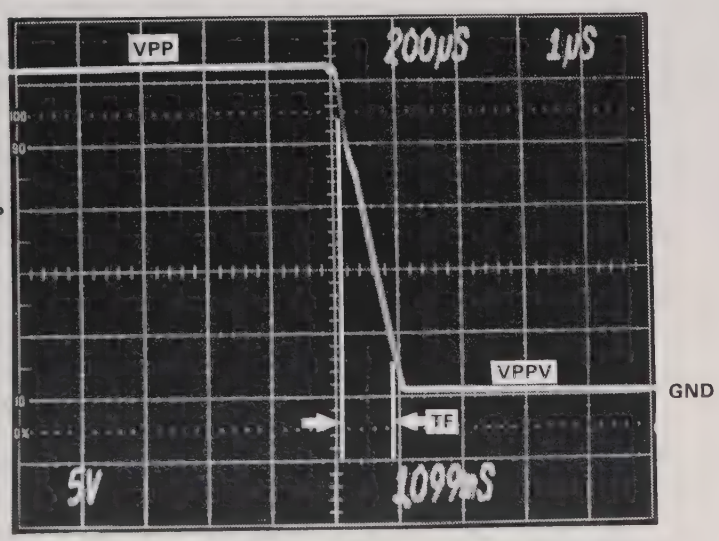
SCALE | SHEET 2/2

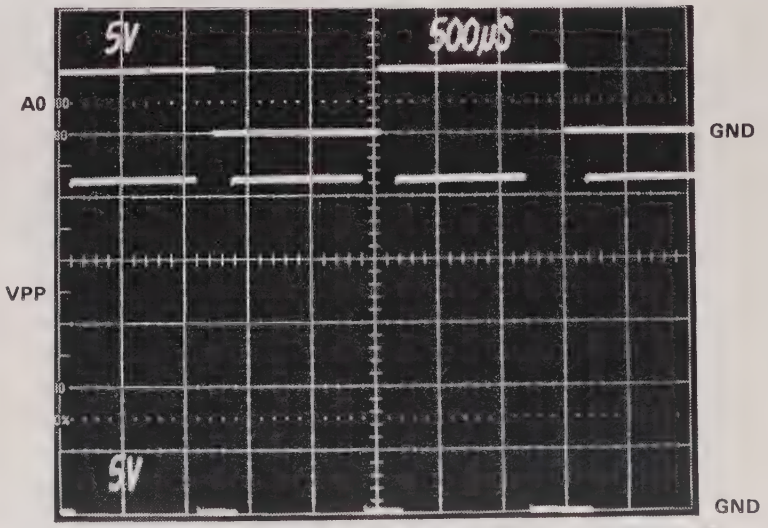


1



2





10-960-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.4	12.0	12.6	V	
	VOP					NA
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0		1.0	V	
	VBB	-5.25	-5.0	-4.75	V	Not Shown
	VDD	11.4	12.0	12.4	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5		2.0	µs	
	TF	0.5		2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 23.*
2. *Load RAM with $01 for Family 24, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address. All 100 loops are performed, and the device is read and verified after all 100 loops.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.T.Z.	11/82
	C	ECN #4831		KH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 23, 24

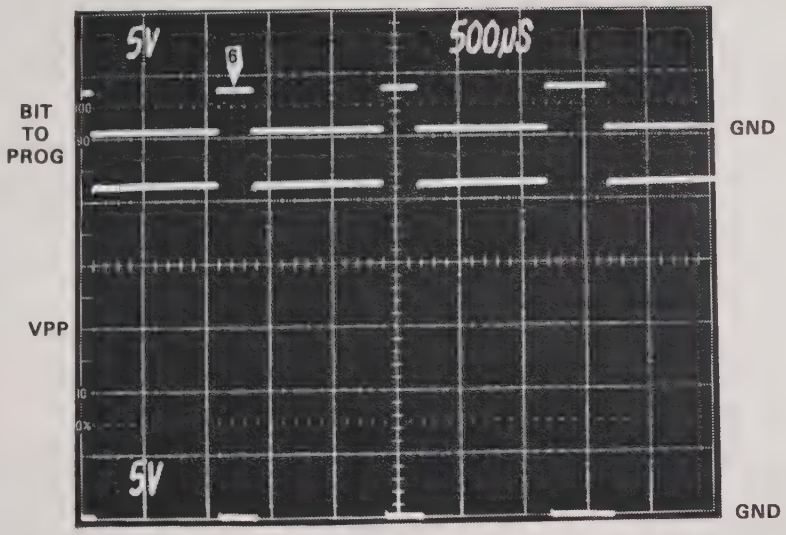
DRAWN BY:

CHECKED BY:

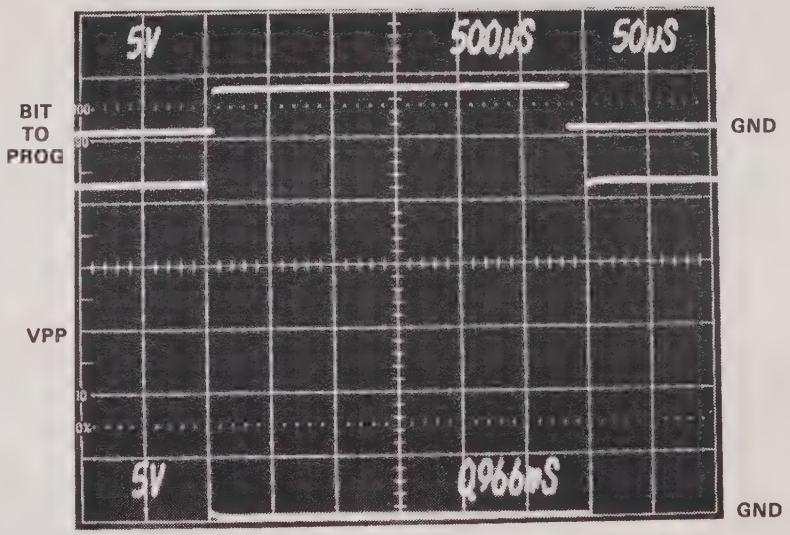
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


5V
500µS
6
BIT
TO
PROG
GND
VPP
5V
GND

5


5V
500µS
50µS
BIT
TO
PROG
GND
VPP
5V
0.966mS
GND

6

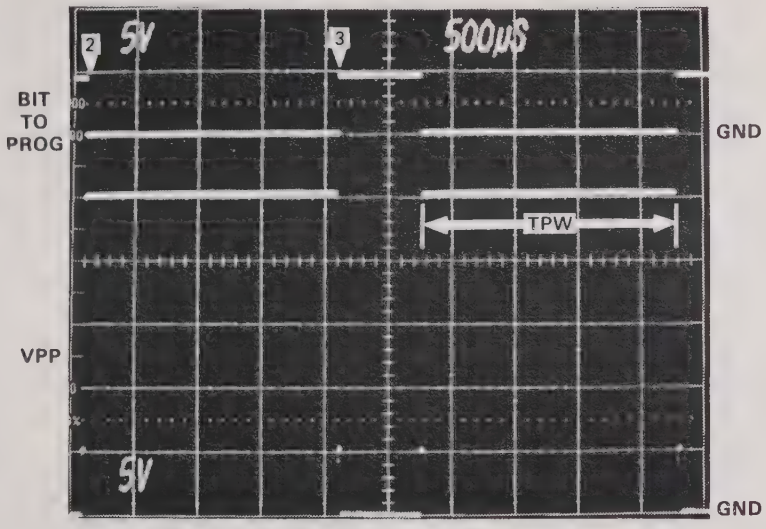
10-950-0059

REVISIONS

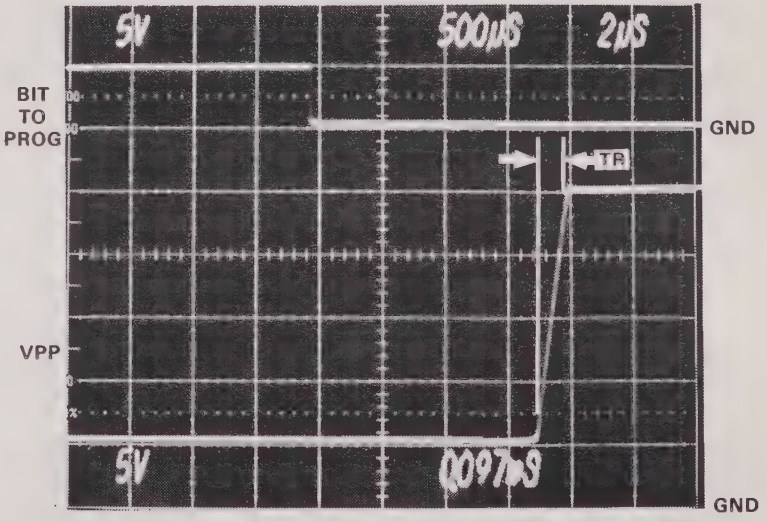
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		JCH	5/83

DATA I/O ISSAQUAH, WA

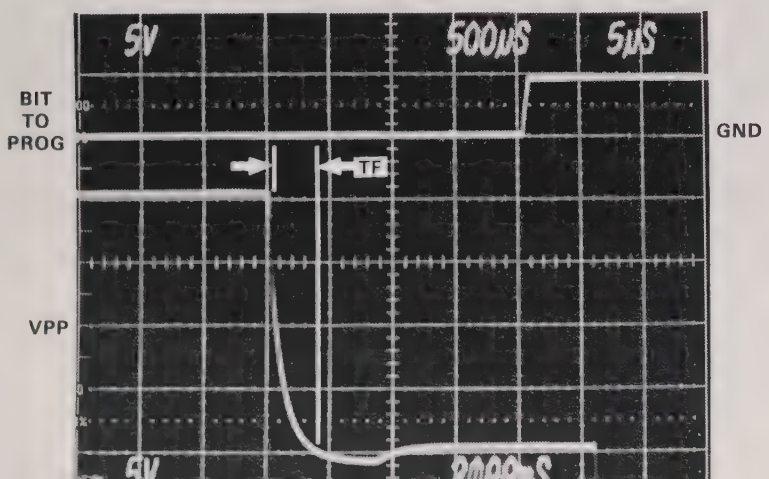
TITLE: TIMING DIAGRAM FAMILY CODES 23, 24	DRAWN BY:	
	CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

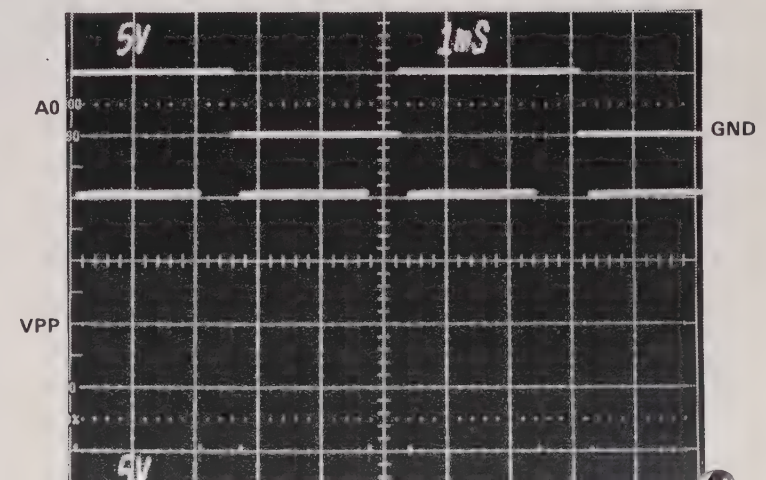


1



2





10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	1.9	2.0	2.1	ms	
	TR	0.5		2.0	µs	
	TF	0.5		5.0	µs	
	Reject		20		Loops	See Note 3
	Overprogram		5		Loops	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 25.*
2. *Load RAM with $01 for Family 26, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *A loop is defined as one complete pass from Address 0 to maximum device address applying one pulse at each address. A read and verify is done after each loop, and when the device verifies, 5 more loops are applied.*

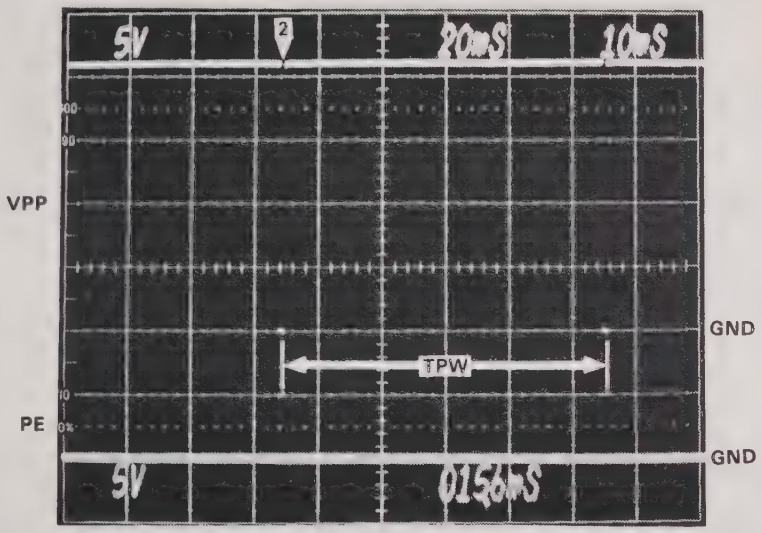
10-950-0059

REVISIONS

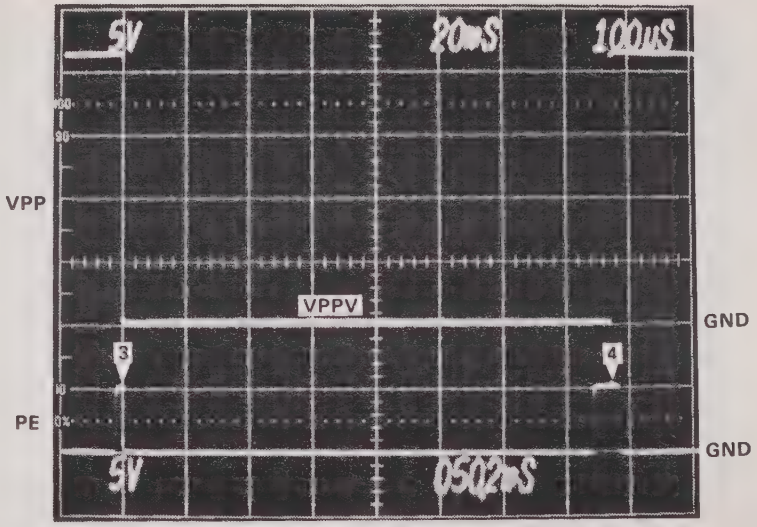
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		XA	5/83

DATA I/O ISSAQUAH, WA

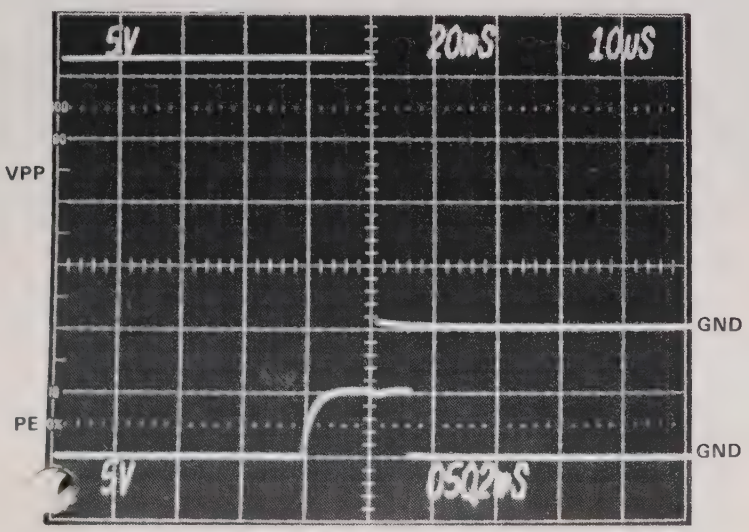
TITLE: TIMING DIAGRAM FAMILY CODES 25, 26	DRAWN BY: EF CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/1


5V
2
20mS
10uS
VPP
GND
TPW
PE
GND
5V
0156mS

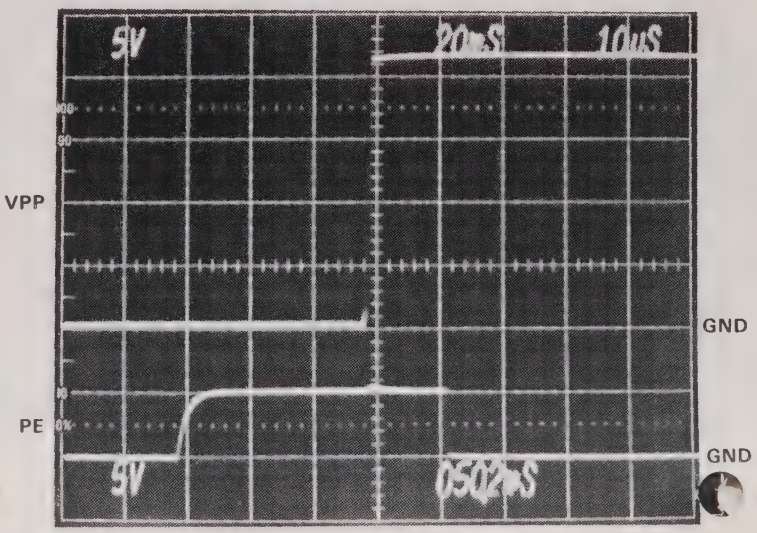
1


5V
20mS
100uS
VPP
VPPV
GND
3
4
PE
GND
5V
0502mS

2


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS

3


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.00	6.00	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	0.0	0.0	0.8	V	
	TPW	48	50	52	ms	
	TR	50			ns	
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 27.*
2. *Load RAM with $01 for Family 28, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*

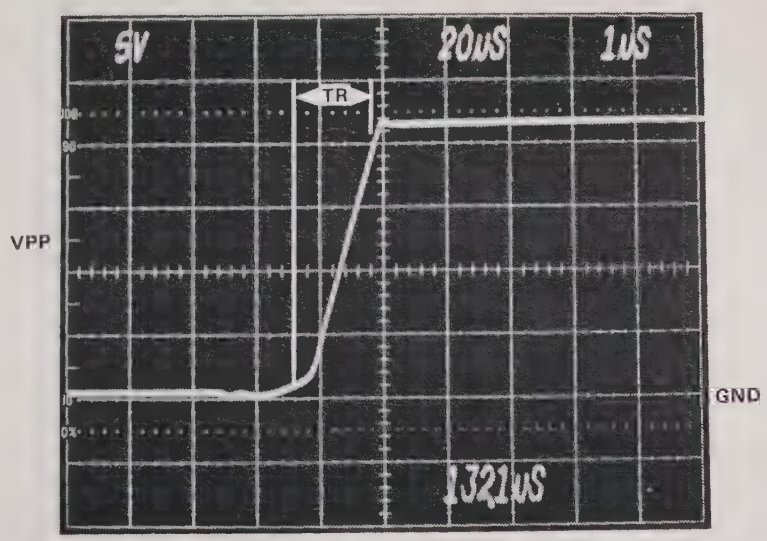
10-950-0059

REVISIONS

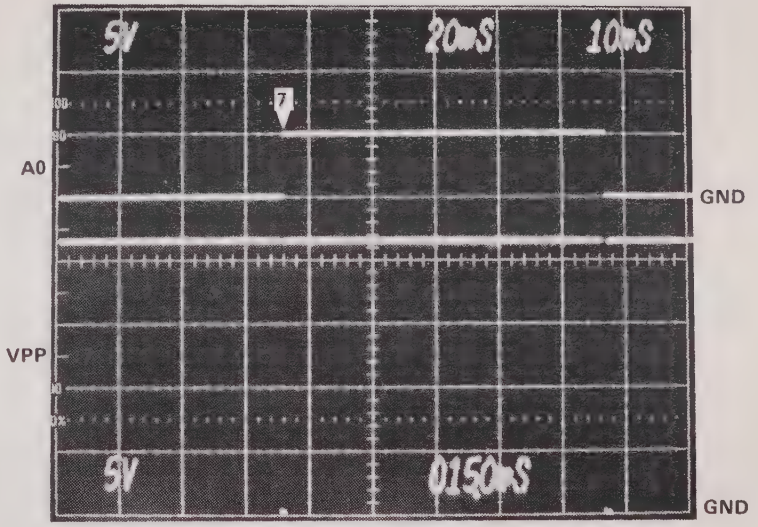
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		[illegible]	11/82
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

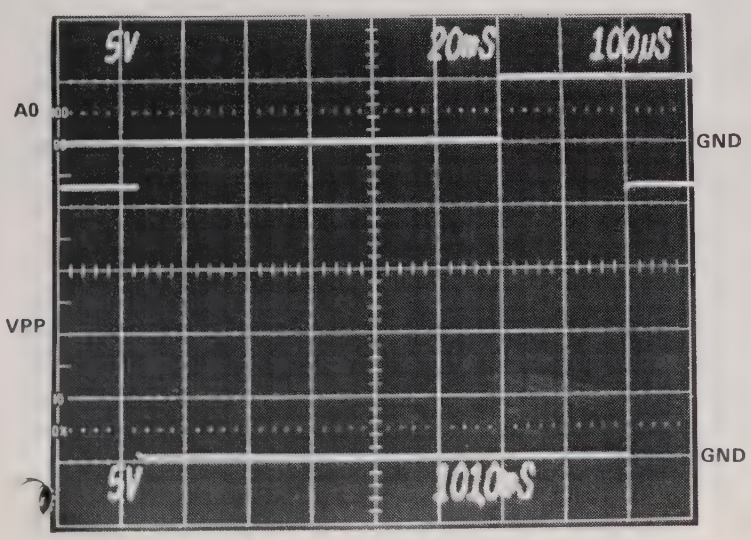
TITLE: TIMING DIAGRAM FAMILY CODES 27, 28		DRAWN BY: ES CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5V
20uS
1uS
TR
VPP
GND
1321uS

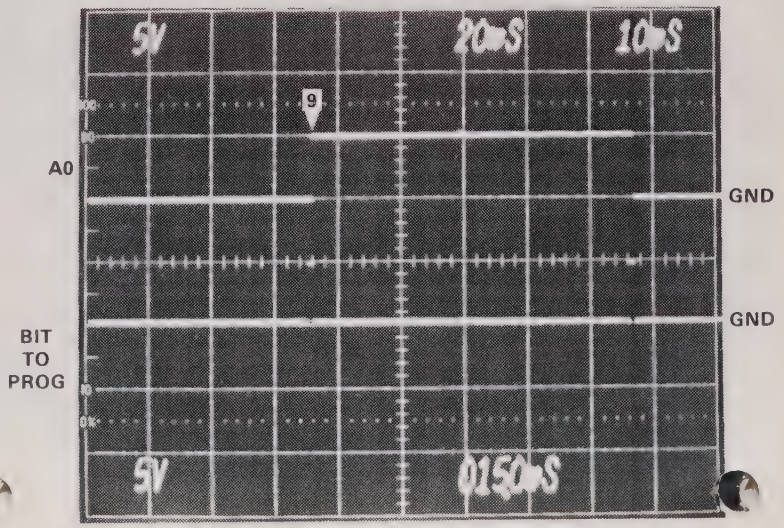
5


5V
20mS
10mS
7
A0
GND
VPP
5V
0150mS
GND

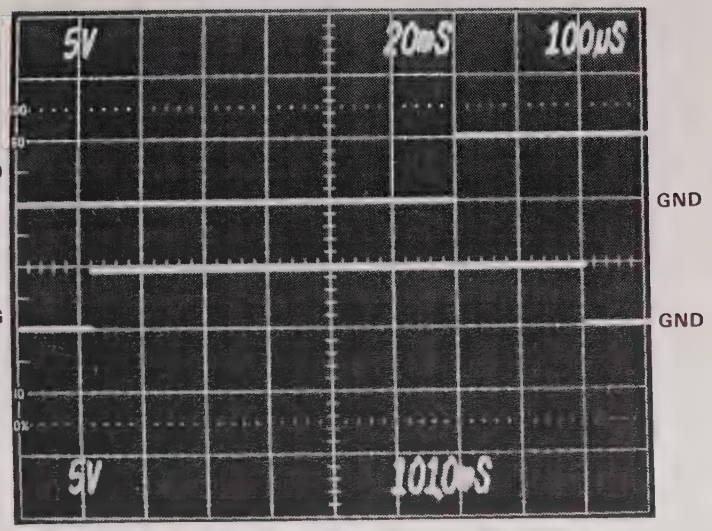
6


5V
20mS
100uS
A0
GND
VPP
GND
5V
1010mS

7


5V
20mS
10mS
9
A0
GND
GND
BIT
TO
PROG
5V
0150mS

8



9

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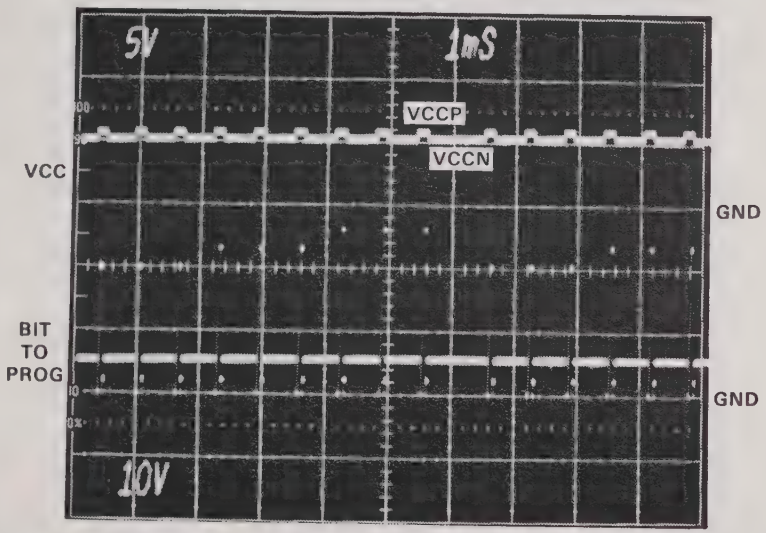
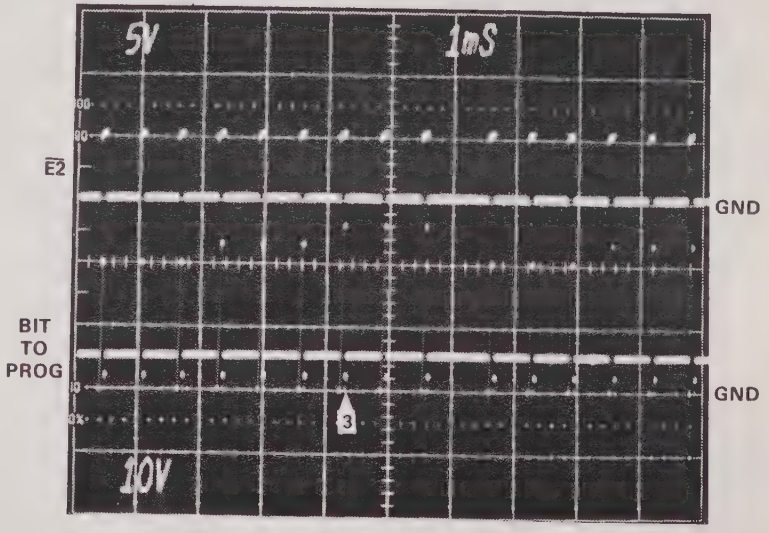
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		X.J	5/83

DATA I/O ISSAQUAH, WA

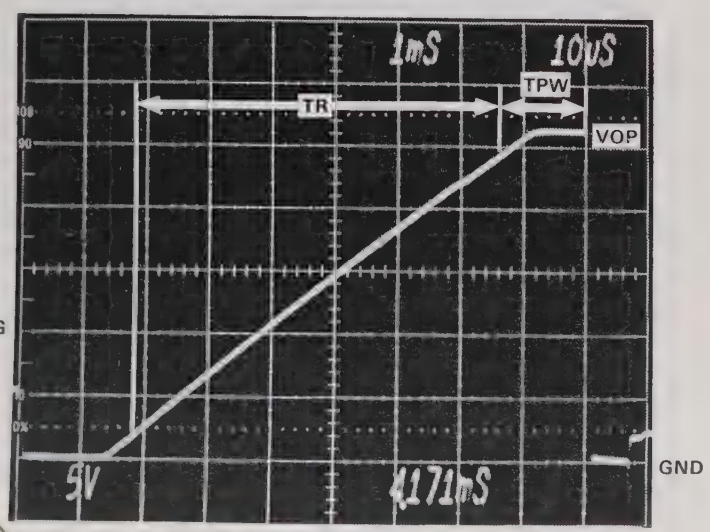
TITLE: TIMING DIAGRAM FAMILY CODES 27, 28		DRAWN BY: ES CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2



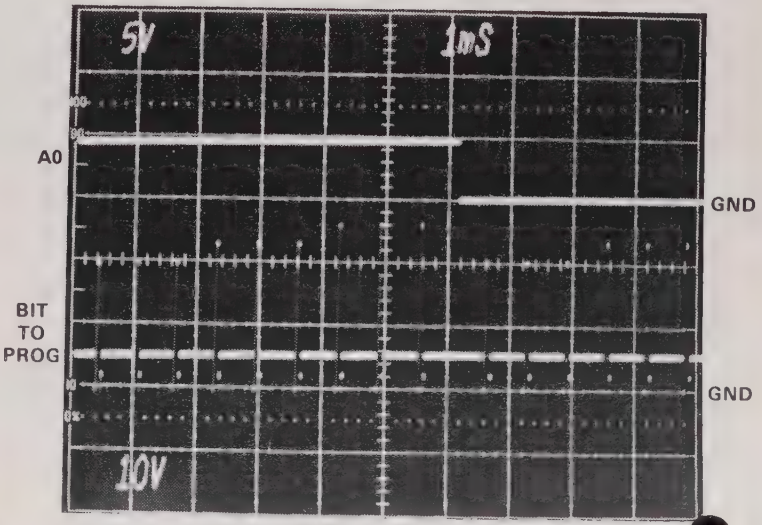
1



2



3



4

10-960-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.4	5.5	5.6	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	TPW	10		40	µs	See note 3
	TR	42	52	69	µs	See note 4
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	17.9	18.9	19.9	V	701-1655/TP4
	Low Load	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.6	5.6	6.6	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 29.*
2. *Load RAM with $01 for Family 30.*
3. *This is measured at the 90% level of the pulse, and all three pulses must meet this specification.*
4. *This is measured from 10% to 90% on the 26V pulses.*

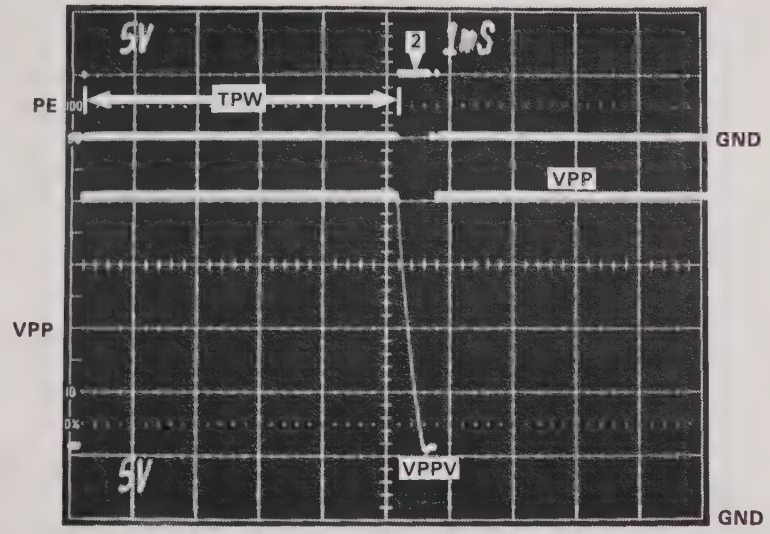
10-950-0059

REVISIONS

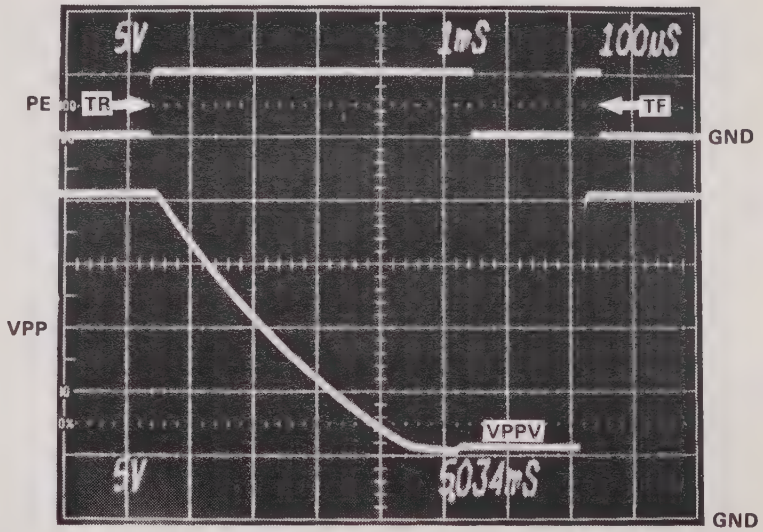
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJ3	11/5/2
	C	ECN #4831		JR	5/6/

DATA I/O ISSAQUAH, WA

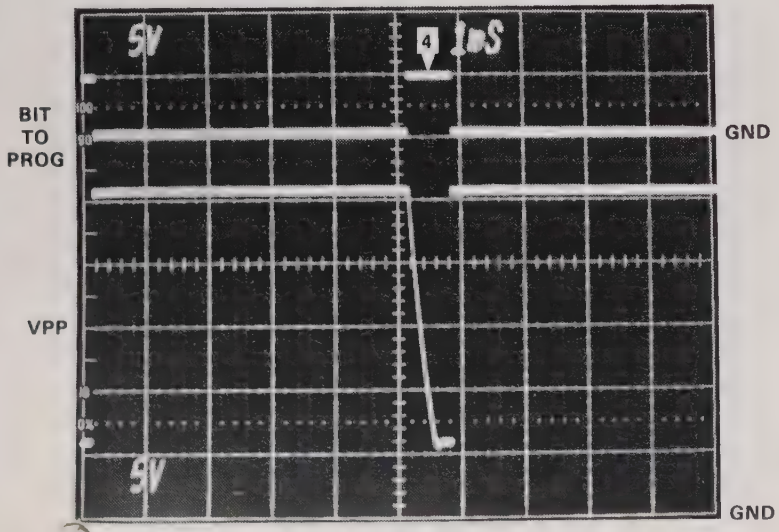
TITLE: TIMING DIAGRAM FAMILY CODES 29, 30		DRAWN BY: EC CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/1


5V
2
1mS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

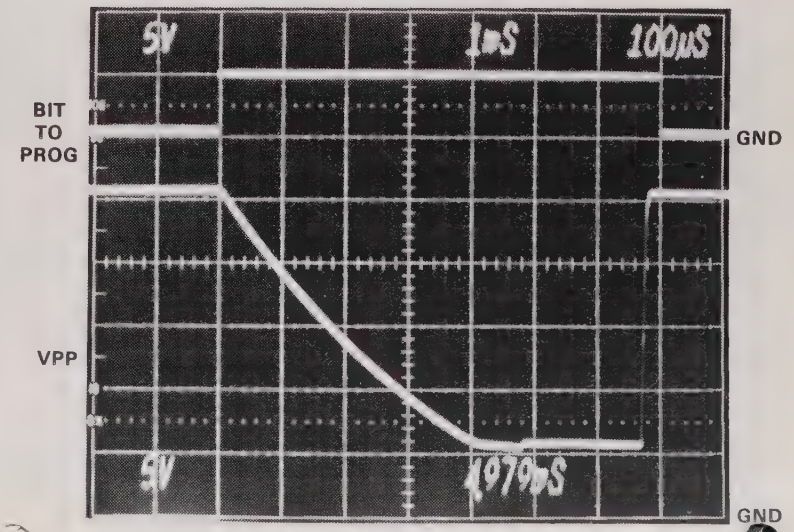
1


5V
1mS
100uS
PE
TR
TF
GND
VPP
VPPV
5V
5034mS
GND

2


5V
4
1mS
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
1mS
100uS
BIT
TO
PROG
GND
VPP
5V
1979mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	4.9	5.0	5.1	ms	
	TR	5			ns	
	TF	5			ns	
	Reject		5		Pulses	
	Overprogram		x		Pulses	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 31.*
2. *Load RAM with $01 for Family 32, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *The number of overprogram pulses is equal to the greatest number of reject pulses applied to any address.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		[illegible]	11/82
	C	ECN #4831		[illegible]	5/83

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 31, 32

DRAWN BY: [illegible]

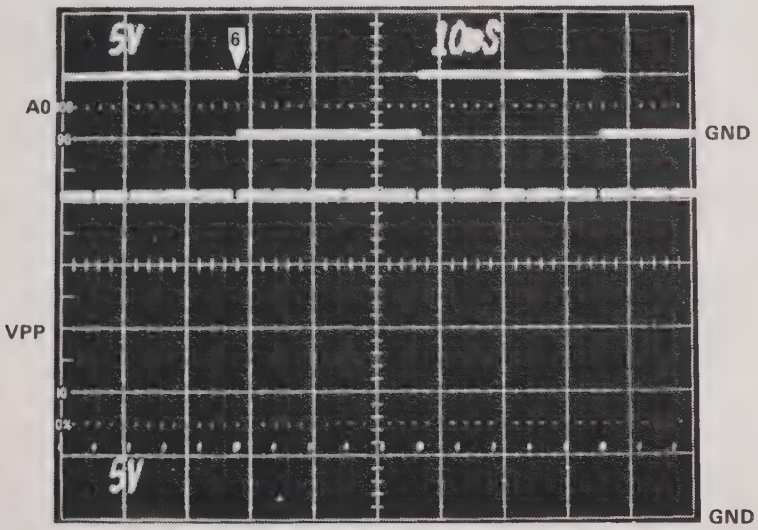
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

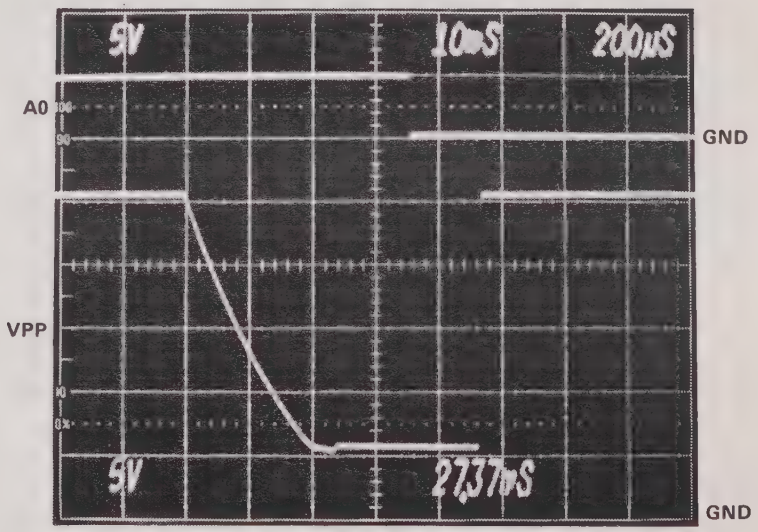
SCALE

SHEET 1/2

10-950-0059


5V
6
10mS
A0
GND
VPP
5V
GND

5


5V
10mS
200µS
A0
GND
VPP
5V
27.37mS
GND

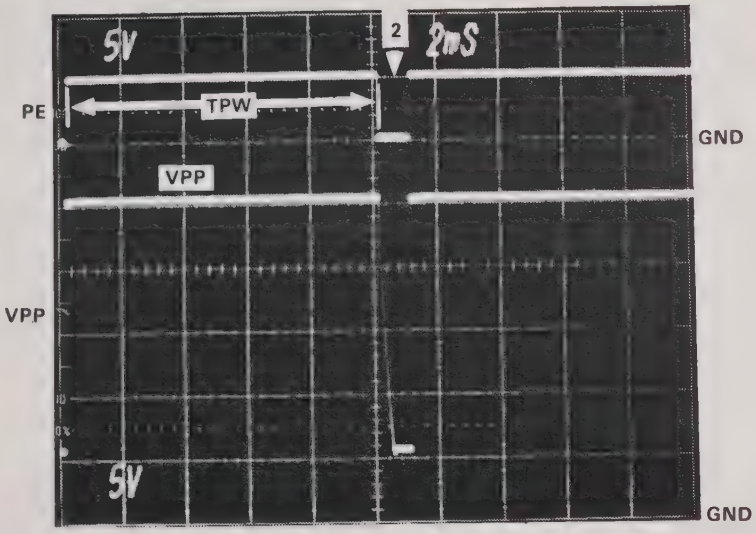
6

10-950-0059

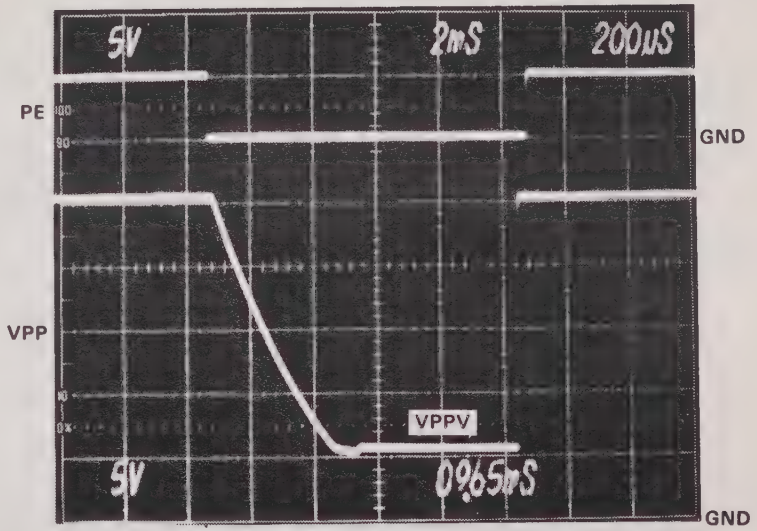
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.B.	11/82
	C	ECN #4831		J.H.	6/85

DATA I/O ISSAQUAH, WA

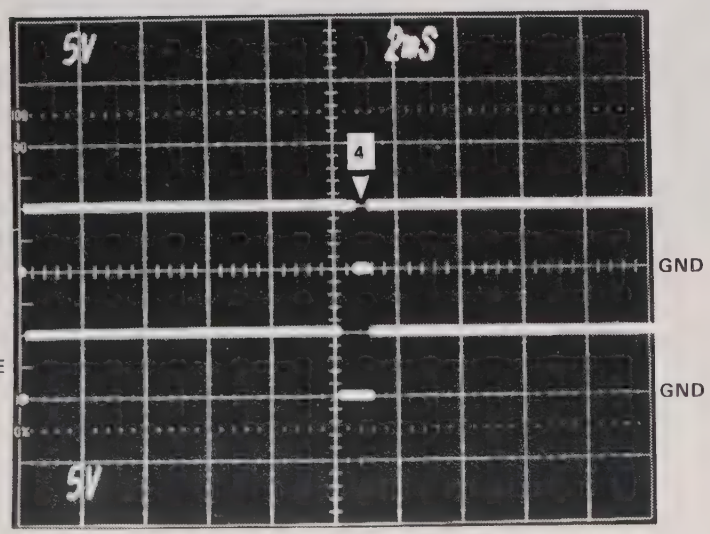
TITLE: TIMING DIAGRAM FAMILY CODES 31, 32		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
2
2mS
PE
TPW
GND
VPP
VPP
5V
GND

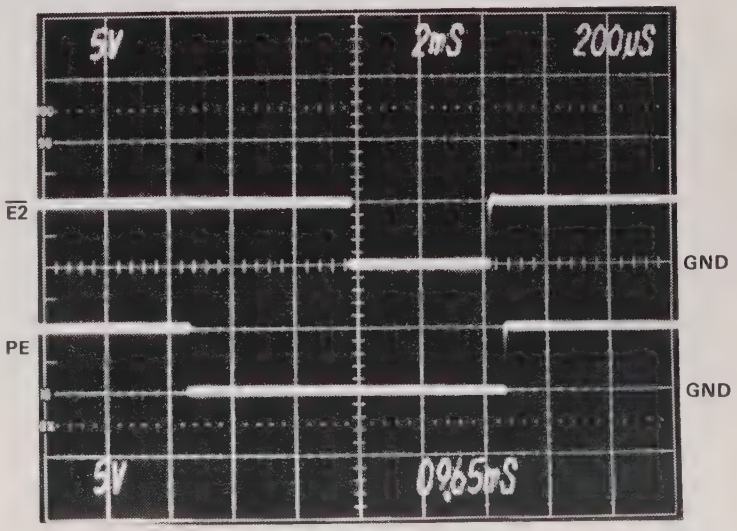
1


5V
2mS
200uS
PE
GND
VPP
VPPV
5V
0%5mS
GND

2


5V
2mS
4
E2
GND
PE
GND
5V

3


5V
2mS
200uS
E2
GND
PE
GND
5V
0%5mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	5			ns	
	TEW	1000			ms	
	TF	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 33.*
2. *Load RAM with $01 for Family 34, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *Photo 11 is the erase waveform.*

10-960-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		[illegible]	11/82
	C	ECN #4831		[illegible]	5/23

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES 33, 34

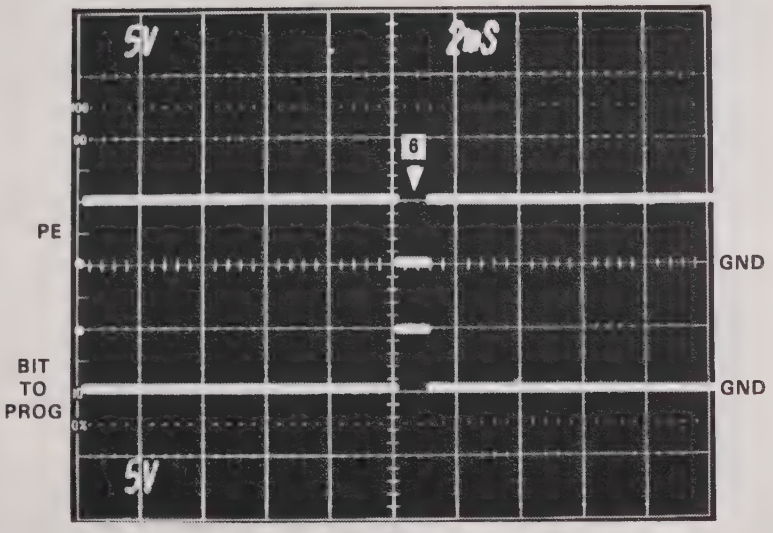
DRAWN BY:

CHECKED BY:

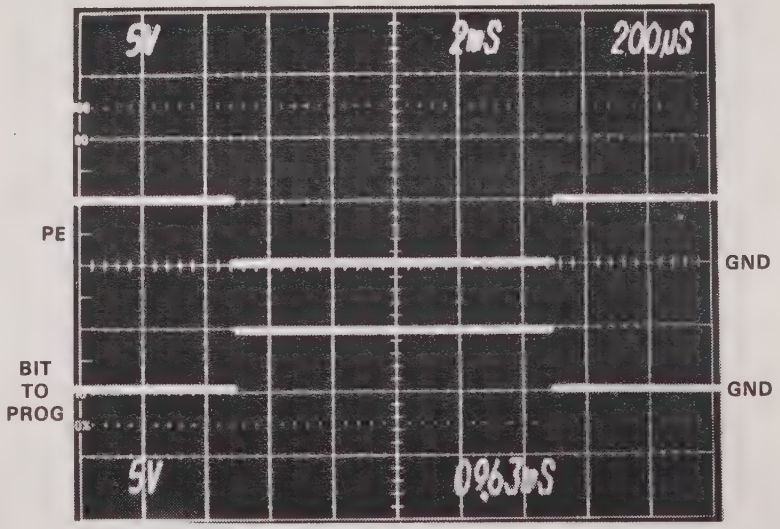
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

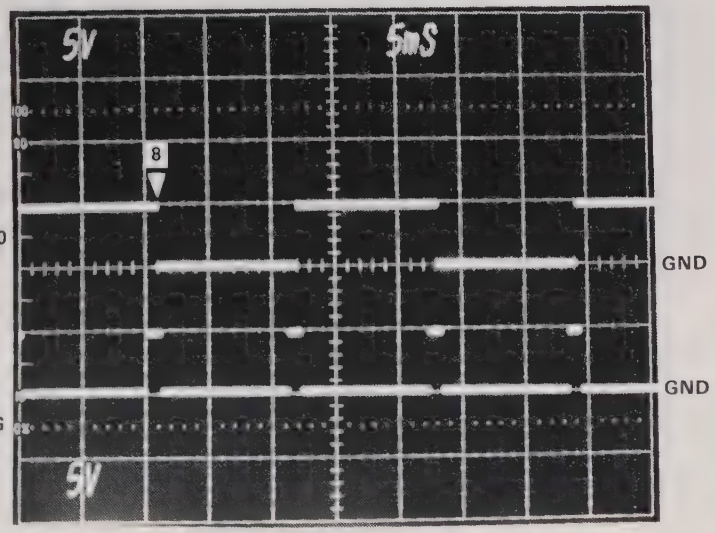
SHEET 1/3


5V
2mS
6
PE
GND
BIT
TO
PROG
GND
5V

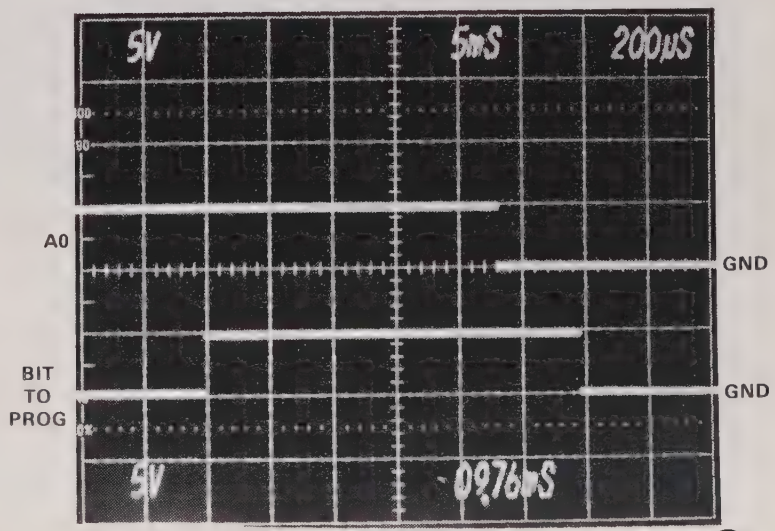
5


5V
2mS
200µS
PE
GND
BIT
TO
PROG
GND
5V
0,63mS

6


5V
5mS
8
A0
GND
BIT
TO
PROG
GND
5V

7


5V
5mS
200µS
A0
GND
BIT
TO
PROG
GND
5V
0,76mS

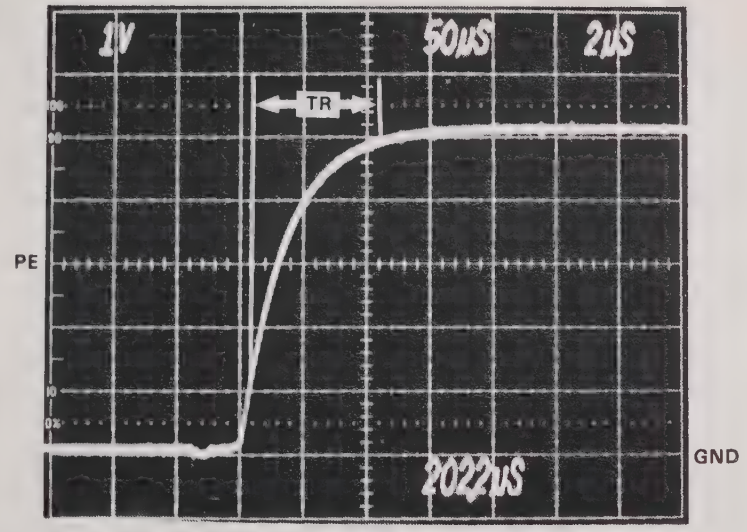
8

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.F.J.	11/82
	C	ECN #4831			

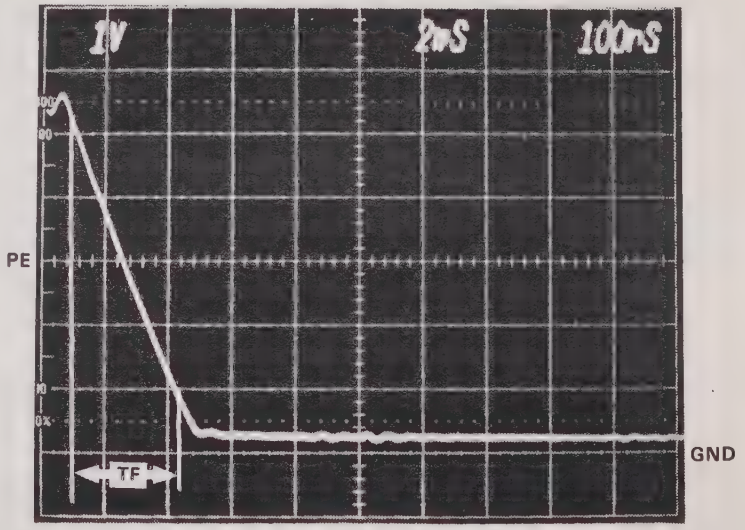
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM			DRAWN BY:
FAMILY CODES 33, 34			CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/3

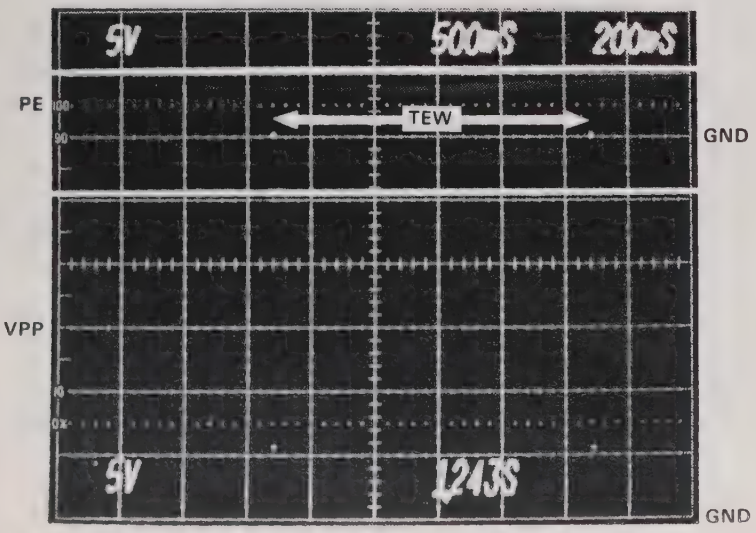
10-950-0059


1V
50uS
2uS
TR
PE
GND
2022uS

9


1V
2mS
100mS
PE
GND
TF

10


5V
500mS
200mS
PE
TEW
GND
VPP
5V
1243S
GND

11

10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		JCH	5/83

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

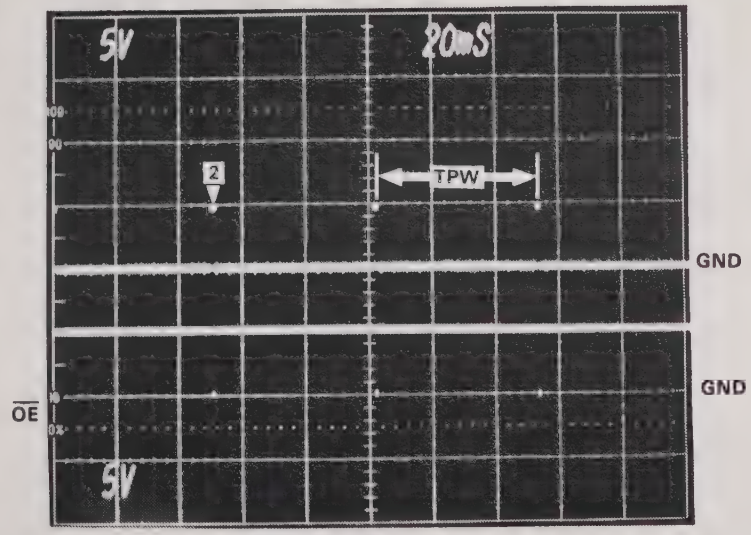
FAMILY CODES 33, 34

DRAWN BY: KEE

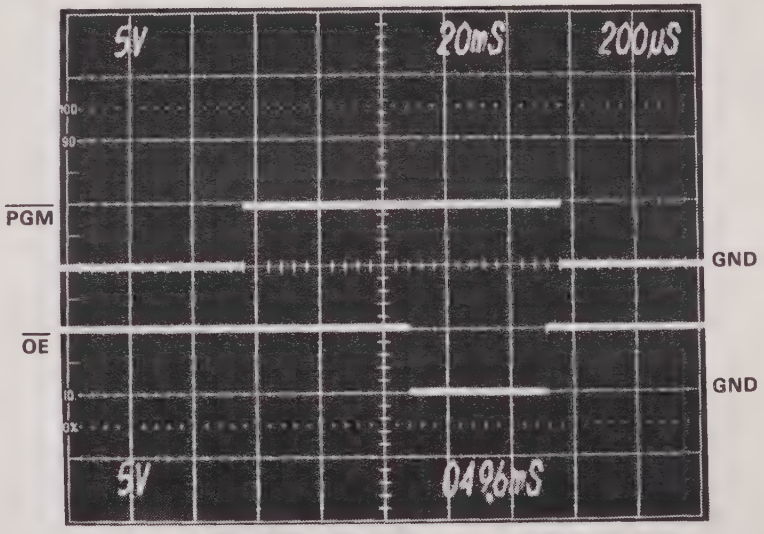
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

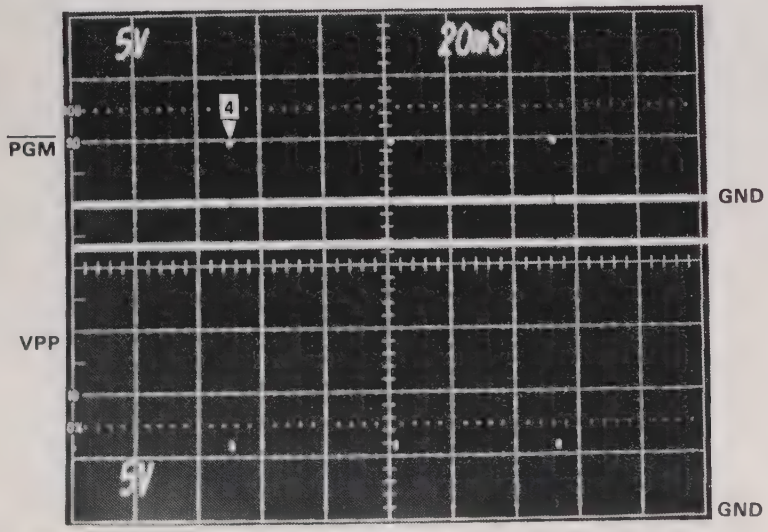
SCALE | SHEET 3/3


5V
20mS
2
TPW
GND
OE
GND
5V

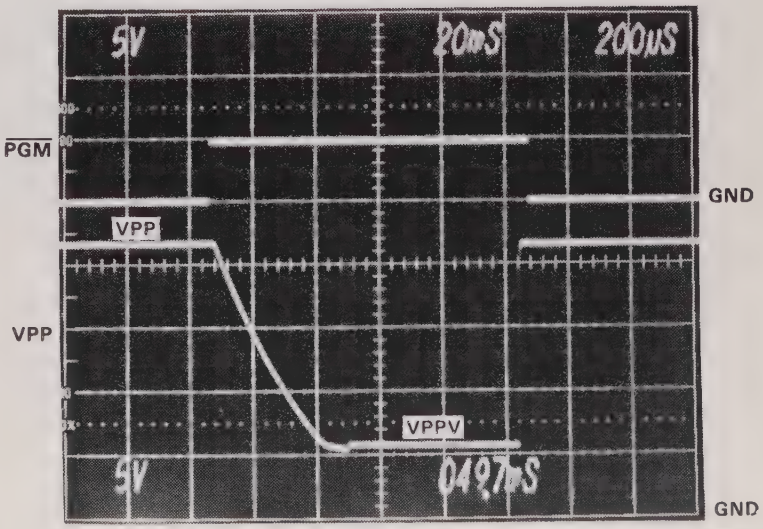
1


5V
20mS
200µS
PGM
GND
OE
GND
5V
049.6mS

2


5V
20mS
4
PGM
GND
VPP
5V
GND

3


5V
20mS
200µS
PGM
GND
VPP
VPP
VPPV
5V
049.7mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	48	50	52	ms	
	TR					NA
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 35.*
2. *Load RAM with $01 for Family 36, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*

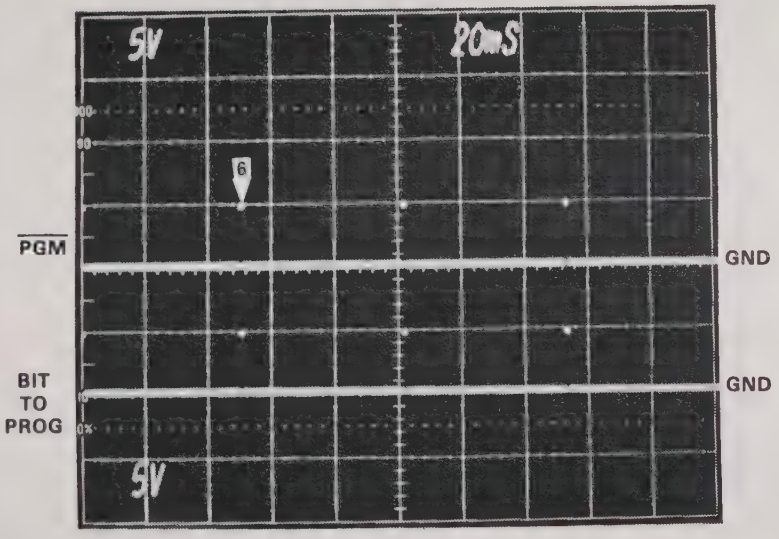
10-950-0059

REVISIONS

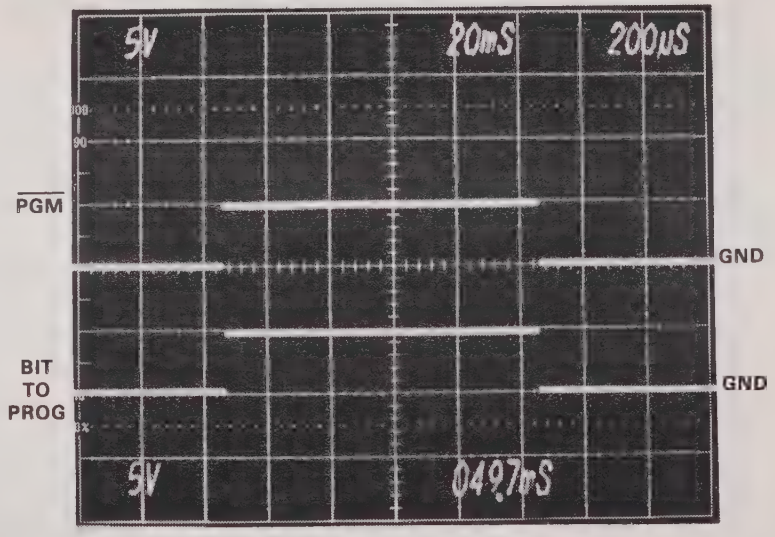
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		[illegible]	11/82
	C	ECN #4831		JA	2/83

DATA I/O ISSAQUAH, WA

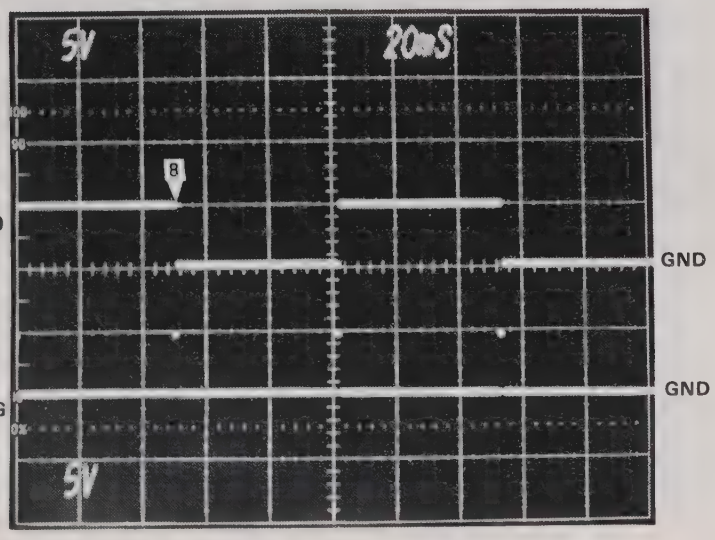
TITLE: TIMING DIAGRAM		DRAWN BY: BG
FAMILY CODES 35, 36		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2



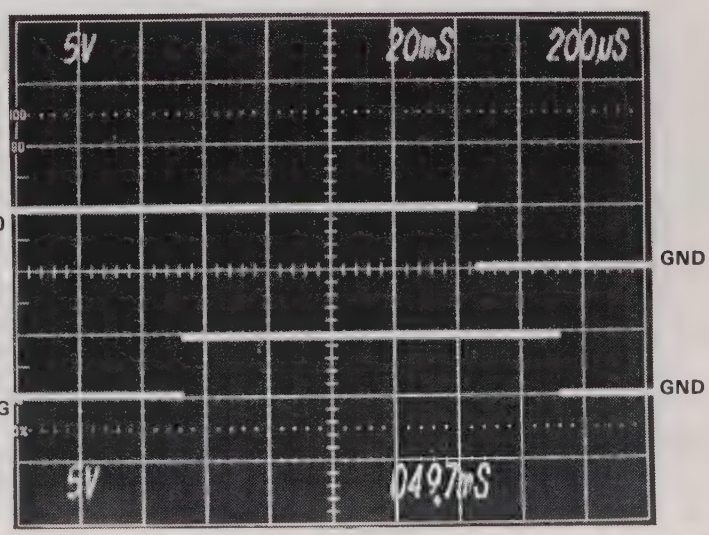
5



6



7



8

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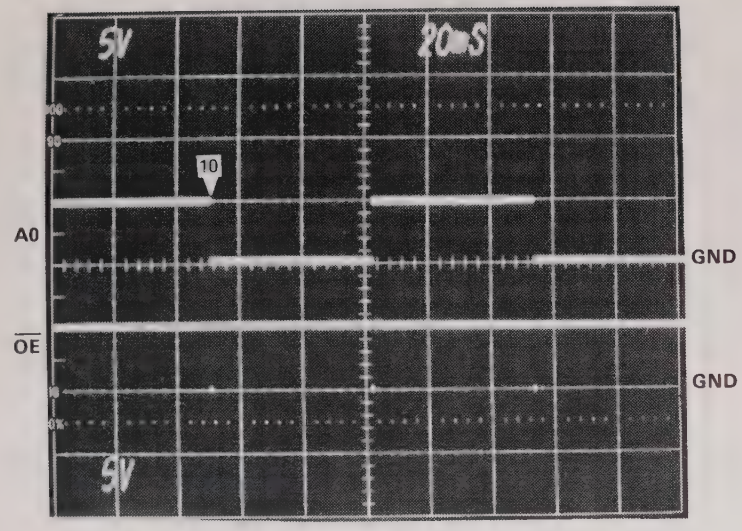
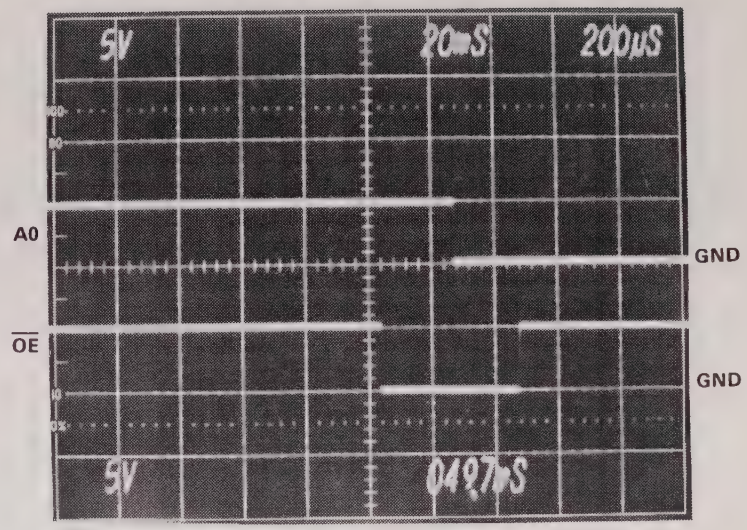


9



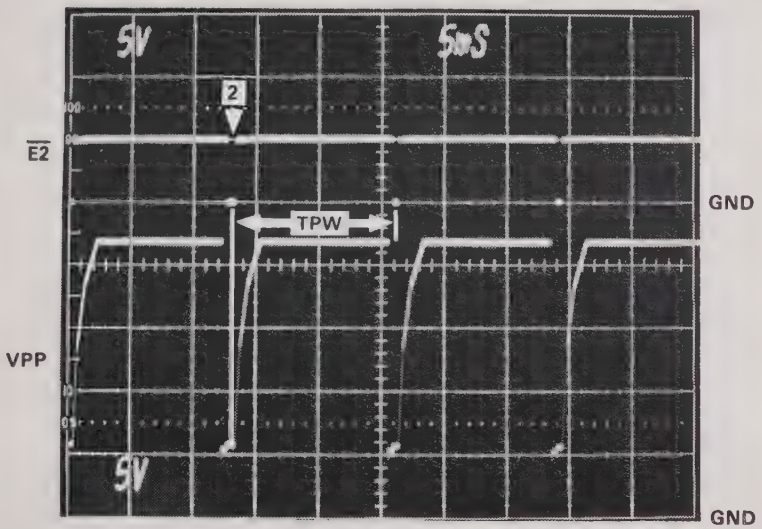
10

10-950-0059

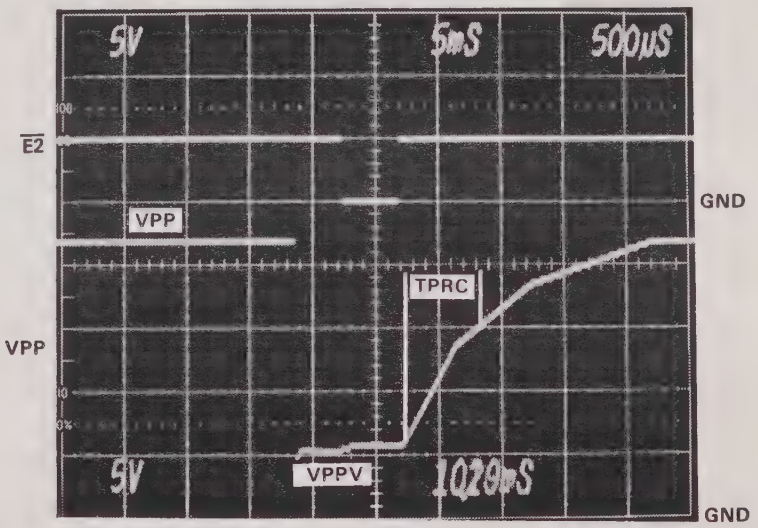
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.T.J.	11/82
	C	ECN #4831		2-	5/83

DATA I/O ISSAQUAH, WA

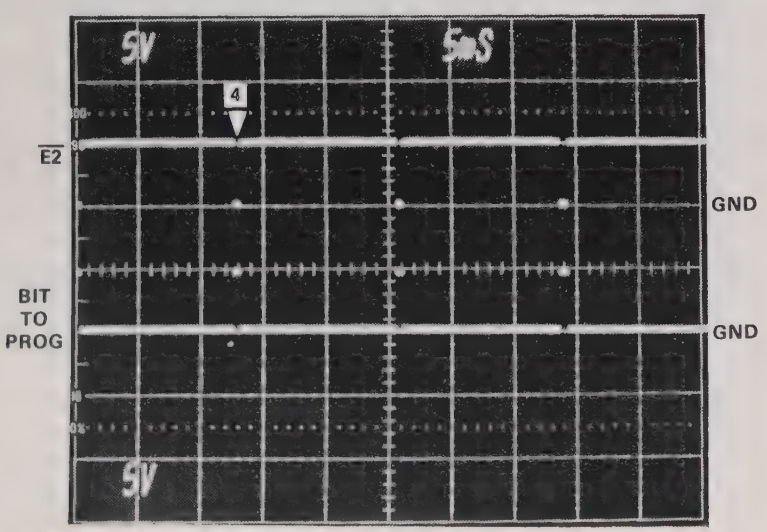
TITLE: TIMING DIAGRAM FAMILY CODES 35, 36	DRAWN BY: BG CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
5mS
2
E2
GND
TPW
VPP
5V
GND

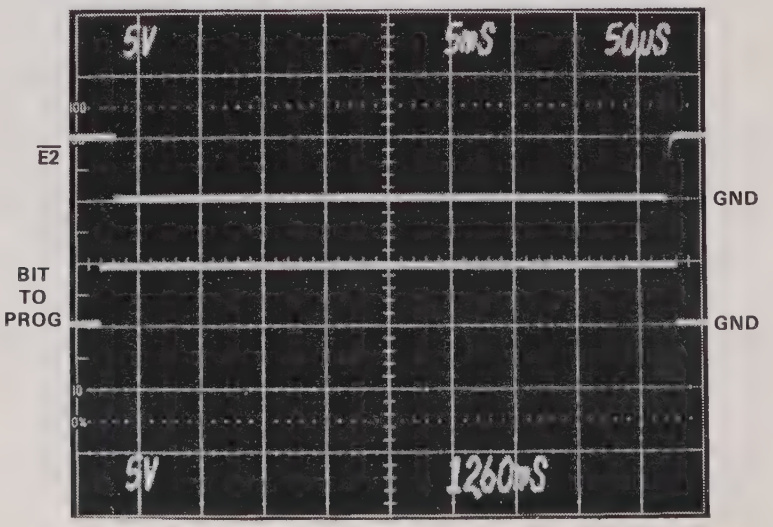
1


5V
5mS
500µS
E2
GND
VPP
TPRC
VPP
5V
VPPV
1029mS
GND

2


5V
5mS
4
E2
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
50µS
E2
GND
BIT
TO
PROG
GND
5V
1260mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VOE	9.0	12.0	15.0	V	
	TPW	9.0	10.0	15.0	ms	
	TPRC	450	600	750	µs	See Note 3
	TF			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 37.*
2. *Load RAM with $01 for Family 38, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *TPRC is measured from 6v to 15.5v.*
4. *Photos 10 and 11 are erase waveforms.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		KA	5/83

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES 37, 38

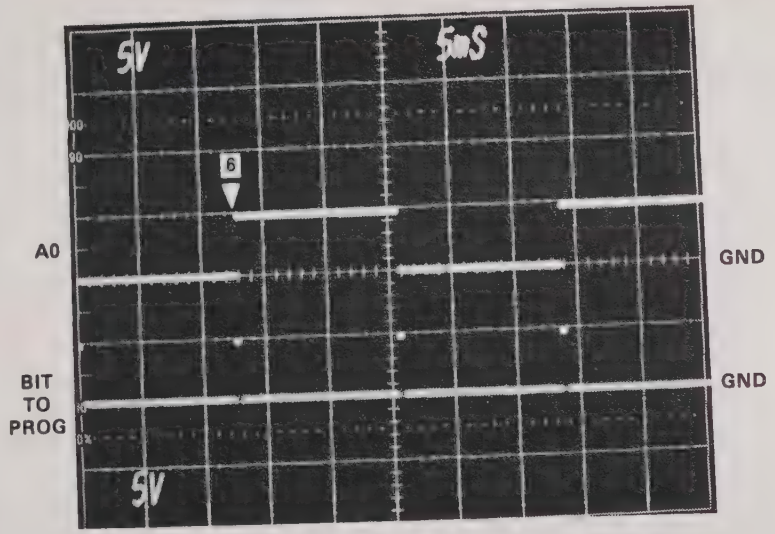
DRAWN BY: KEV

CHECKED BY:

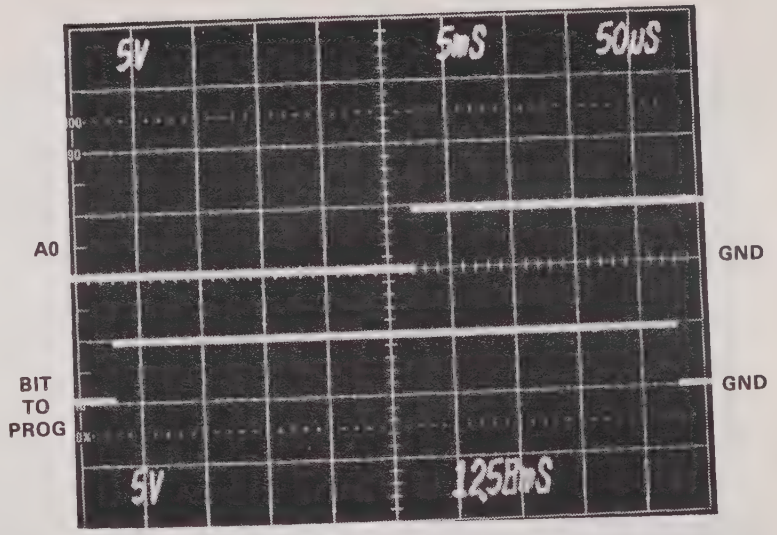
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

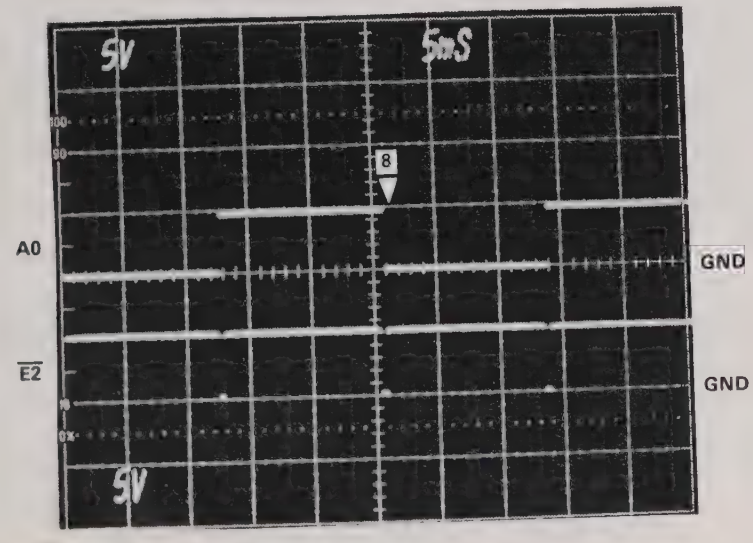
SHEET 1/3


5V
5mS
6
A0
GND
BIT
TO
PROG
GND
5V

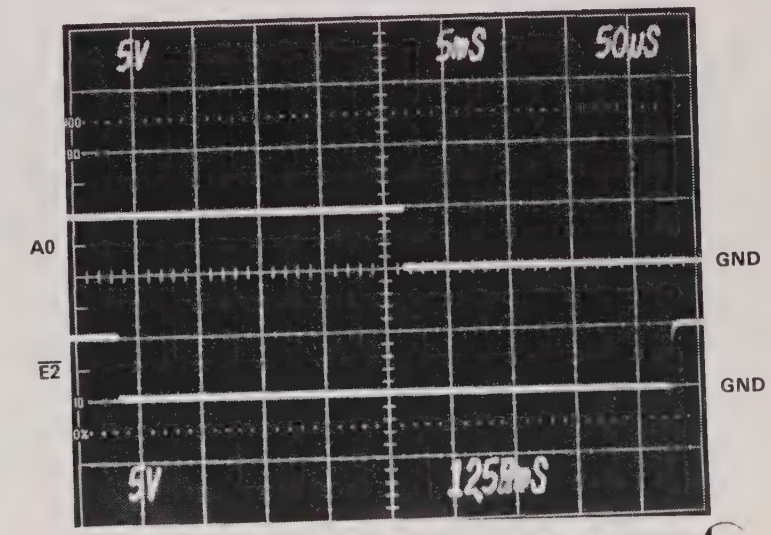
5


5V
5mS
50uS
A0
GND
BIT
TO
PROG
GND
5V
125mS

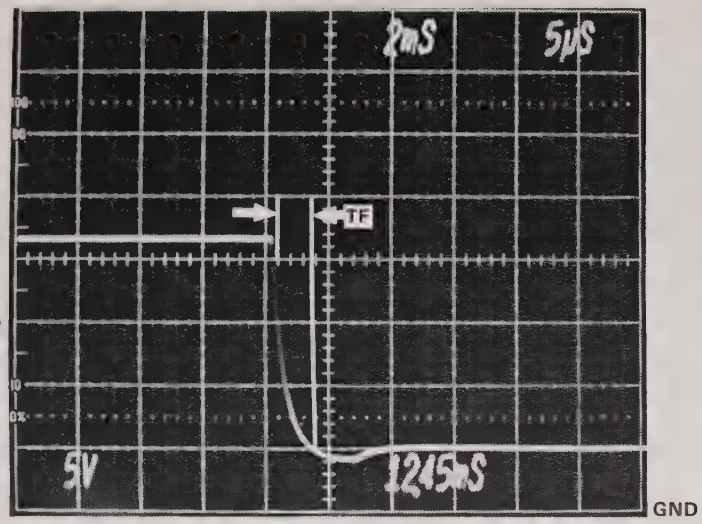
6


5V
5mS
8
A0
GND
E2
GND
5V

7


5V
5mS
50uS
A0
GND
E2
GND
5V
125mS

8



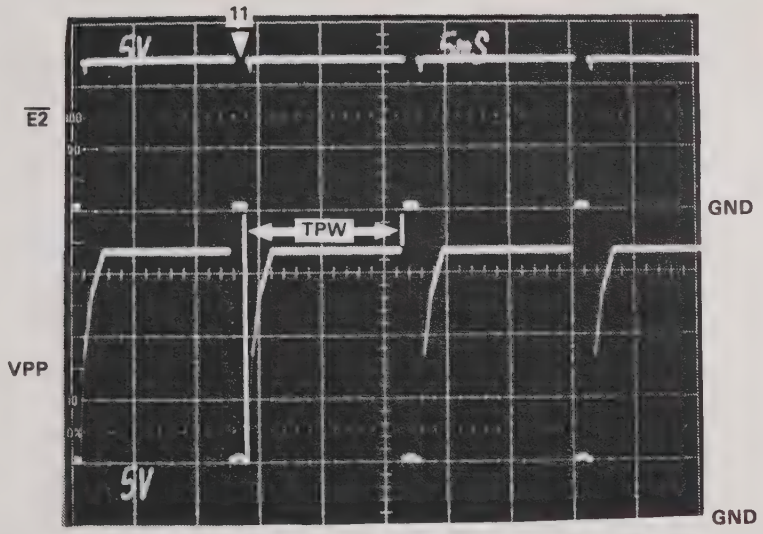
9

10-950-0059

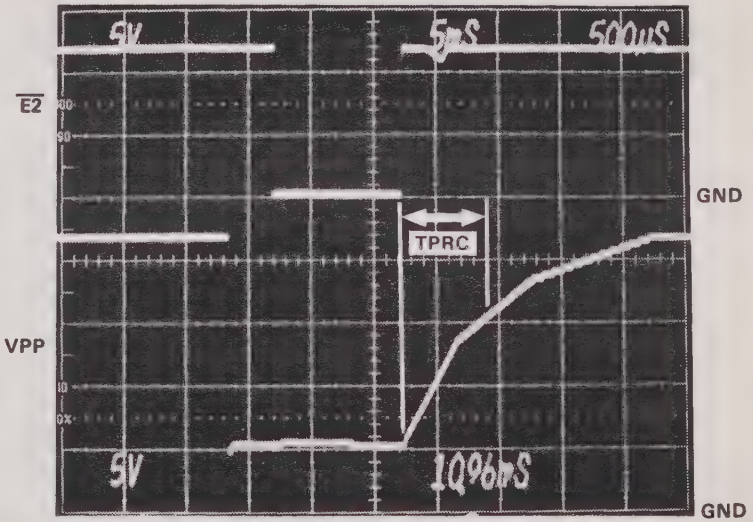
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJJ	11/82
	C	ECN #4831		KA	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 37, 38			DRAWN BY: KEV CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/3


11
5V
5mS
E2
GND
TPW
VPP
5V
GND

10


5V
5mS
500uS
E2
GND
TPRC
VPP
5V
GND

11

10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.3	11/82
	C	ECN #4831		JH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 37, 38

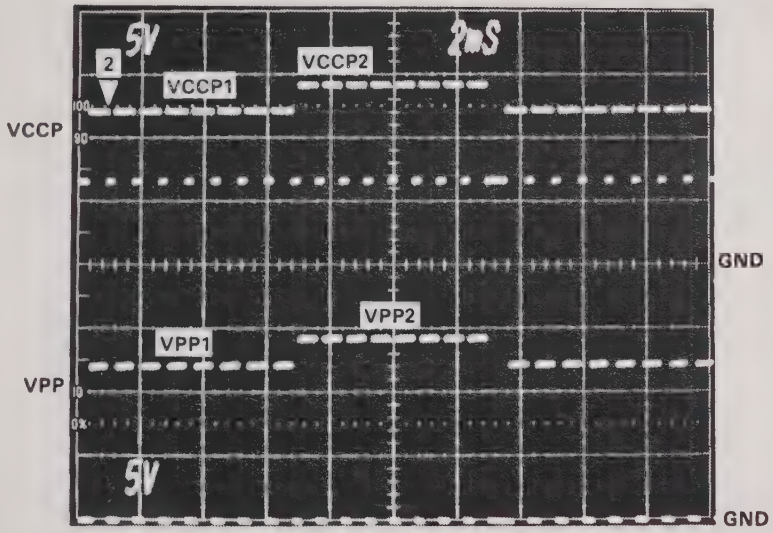
DRAWN BY: KEV

CHECKED BY:

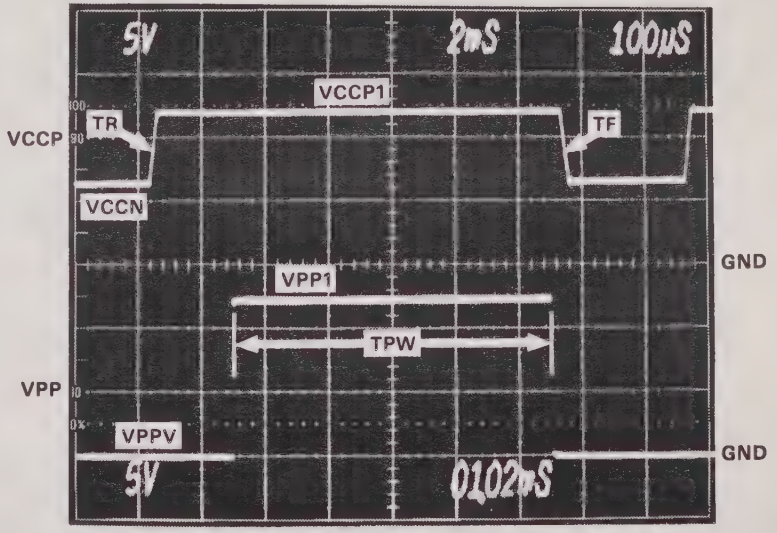
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

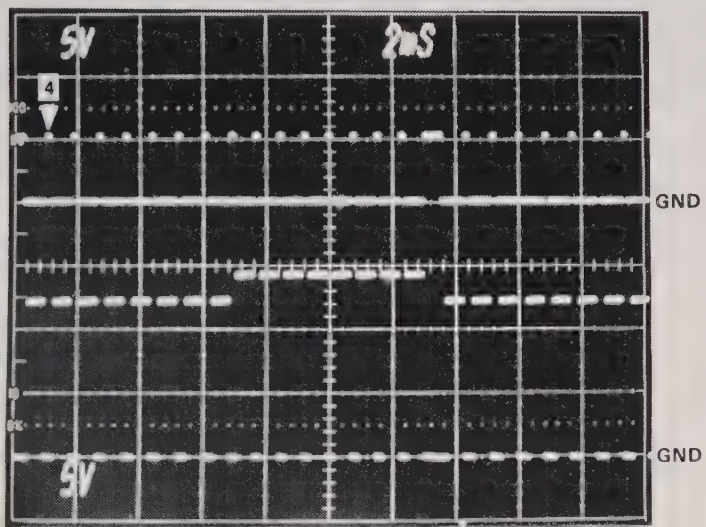
SHEET 3/3

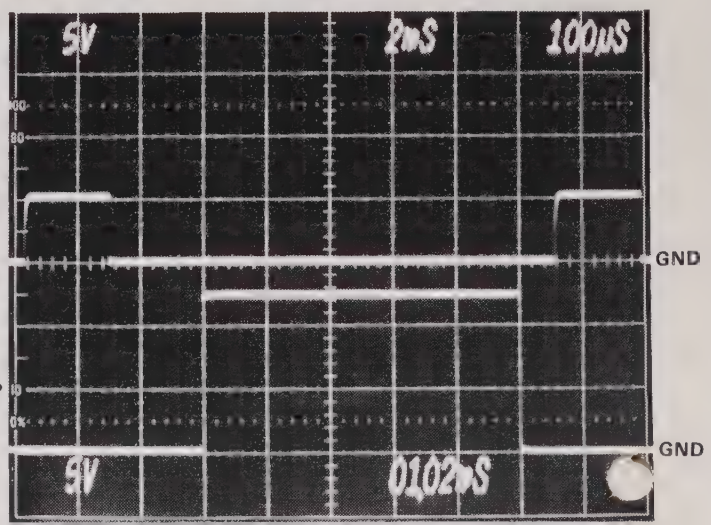

5V
2mS
2
VCCP1
VCCP2
VCCP
GND
VPP2
VPP1
VPP
5V
GND

1


5V
2mS
100µS
VCCP1
VCCP
TR
TF
VCCN
GND
VPP1
TPW
VPP
VPPV
GND
5V
0102mS

2


5V
2mS
4
E3
GND
VPP
GND
5V


5V
2mS
100µS
E3
GND
VPP
GND
5V
0102mS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCN	6.0	6.5	7.0	V	
	VCCP1	11.5	12.0	12.5	V	Pulses 1-8
	VCCP2	13.5	14.0	14.5	V	Pulses 9-16
	VPP1	11.5	12.0	12.5	V	Pulses 1-8
	VPP2	13.5	14.0	14.5	V	Pulses 9-16
	VPPV	0.0		1.0	V	
	VOP1	11.5	12.0	12.5	V	Pulses 1-8
	VOP2	13.5	14.0	14.5	V	Pulses 9-16
	TPW	450	500	550	µs	
	T_R	1.0			µs	
	T_F	1.0			µs	
	Reject		16		Pulses	
	Overprogram		2		Pulses	
1ST PASS VERIFY	VCC	3.9	4.0	4.1	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	6.1	7.1	8.1	V	701-1655/TP4
	Low Load	6.1	7.1	8.1	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	4.0	4.1	4.2	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.7	9.7	10.7	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 39.*
2. *Load RAM with $01 for Family 40.*
3. *V_{CC} is loaded with a 100 Ω, 2 watt resistor.*

10-950-0059

REVISIONS

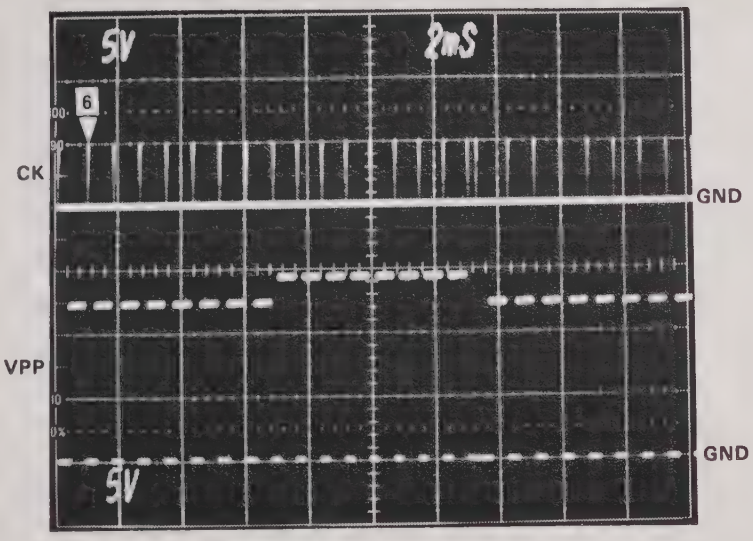
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.T.J.	11/82
	C	ECN #4831		KA	1/8

DATA I/O ISSAQUAH, WA

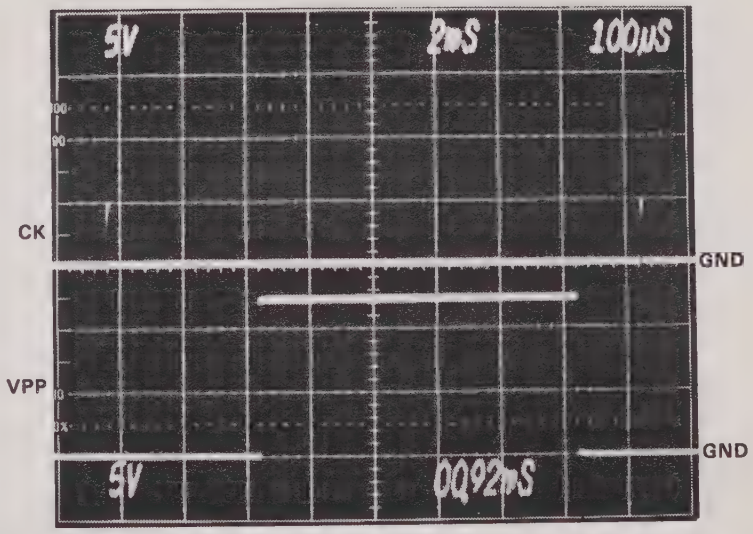
TITLE: TIMING DIAGRAM	DRAWN BY:
FAMILY CODES 39, 40	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

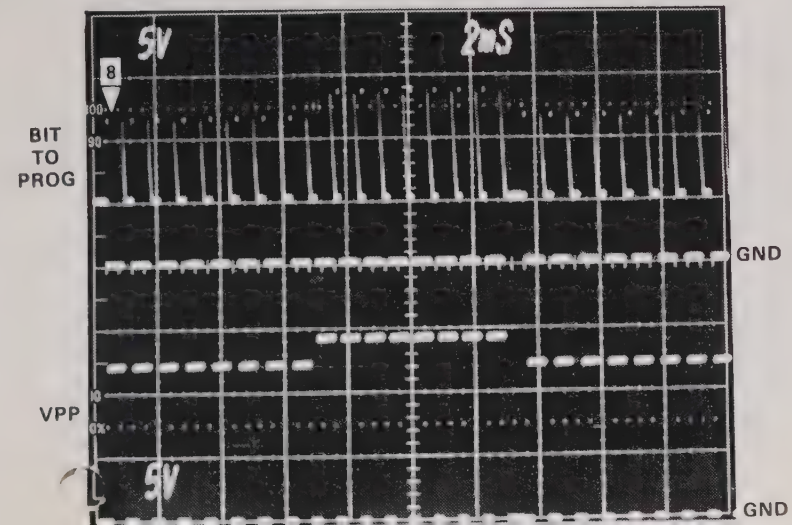
SCALE | SHEET 1/3

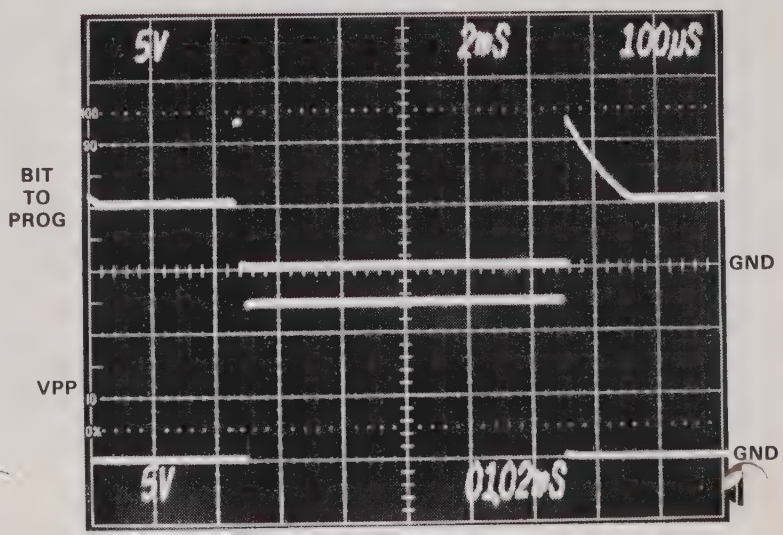

5V
2mS
6
CK
GND
VPP
GND
5V

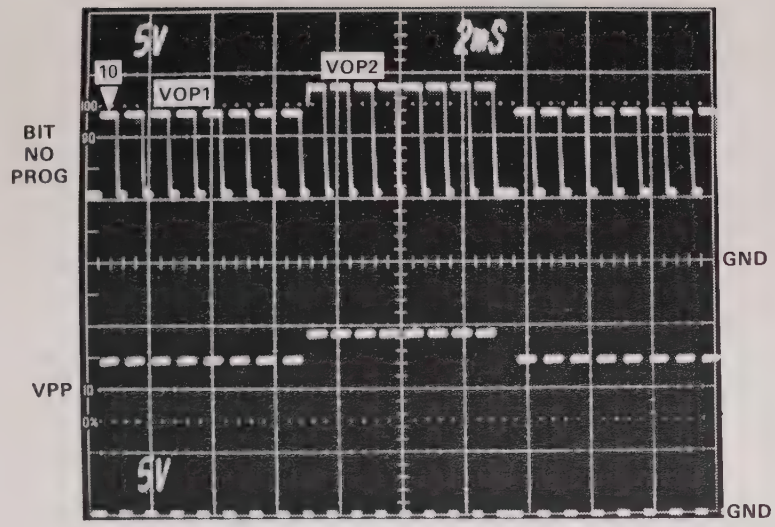
5


5V
2mS
100µS
CK
GND
VPP
GND
5V
0Q92mS

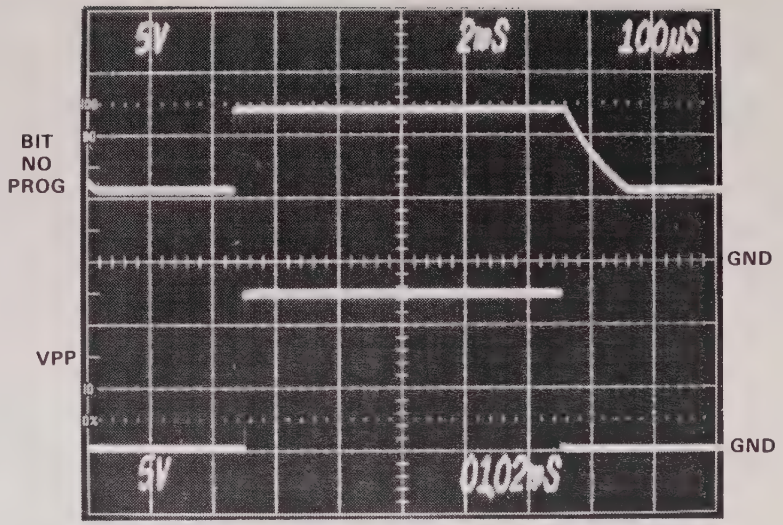
6


5V
2mS
8
BIT
TO
PROG
GND
VPP
5V
GND


5V
2mS
100µS
BIT
TO
PROG
GND
VPP
GND
5V
0102mS



9



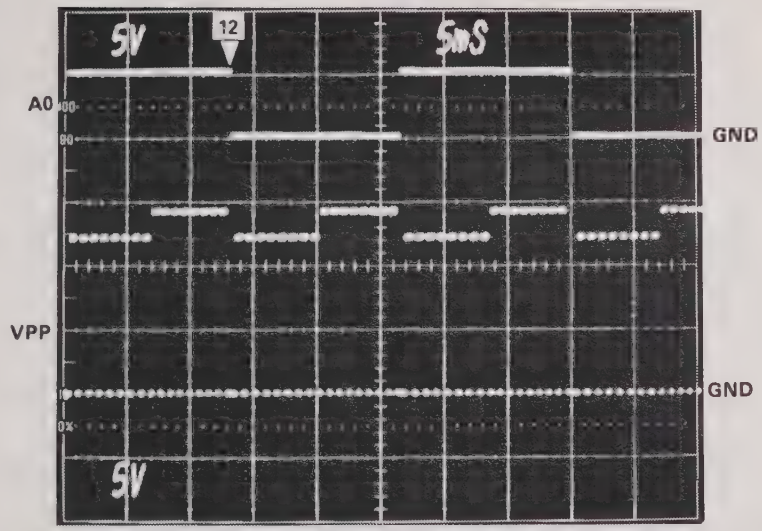
10

10-950-0059

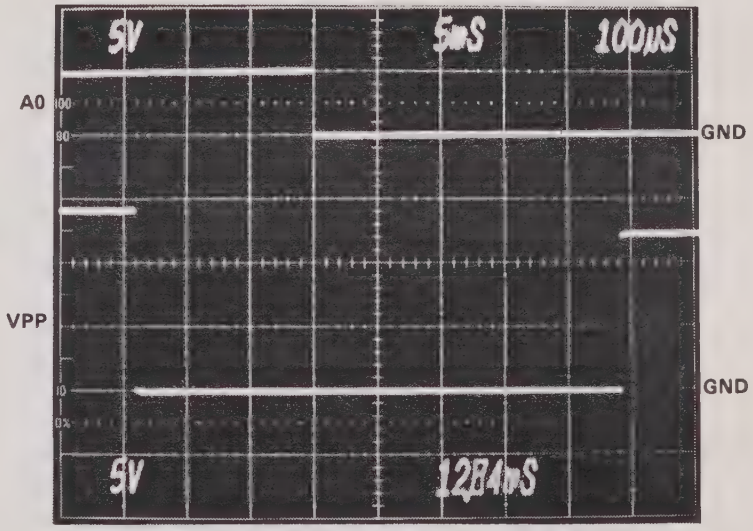
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.T.Z.	11/82
	C	ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 39, 40	DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 2/3



11



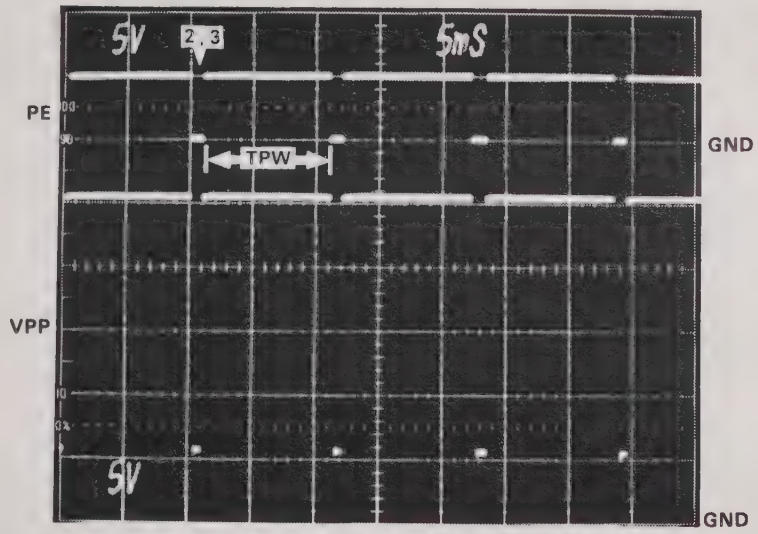
12

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		[illegible]	5/23

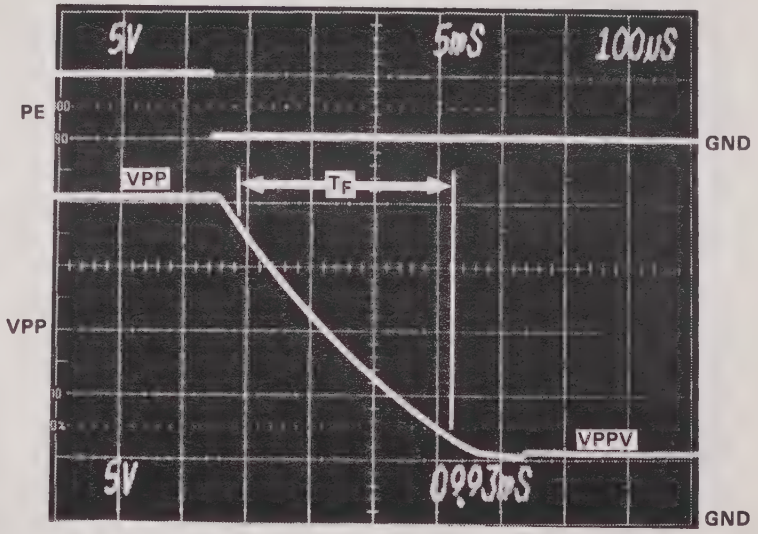
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 39, 40			DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099	
SCALE			SHEET 3/3

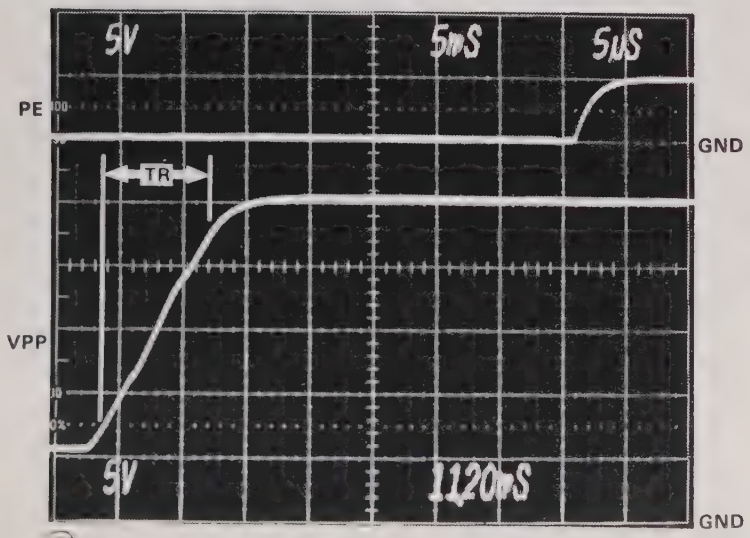
10-950-0059


5V
2, 3
5mS
PE
TPW
GND
VPP
5V
GND

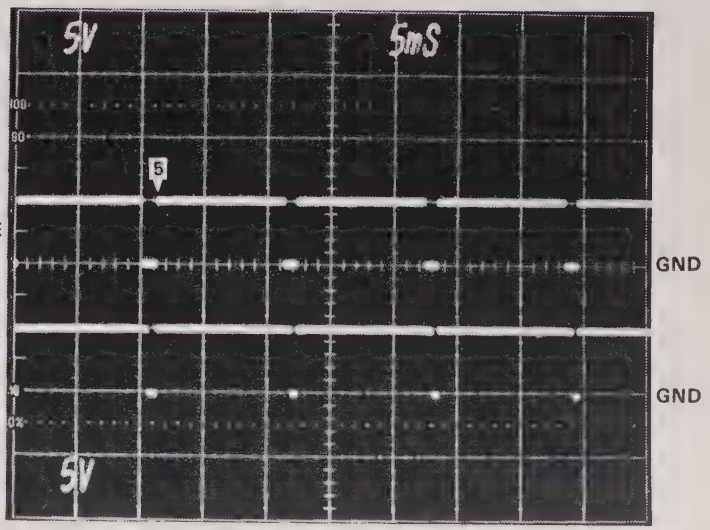
1


5V
5mS
100uS
PE
GND
VPP
TF
VPP
VPPV
5V
0993mS
GND

2


5V
5mS
5uS
PE
GND
TR
VPP
5V
1120mS
GND

3


5V
5mS
5
PE
GND
E2
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	50			ns	
	TEP	98	100	102	ms	
	TF	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 43.*
2. *Load RAM with $01 for Family 44, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *Photo 10 is the erase waveform.*

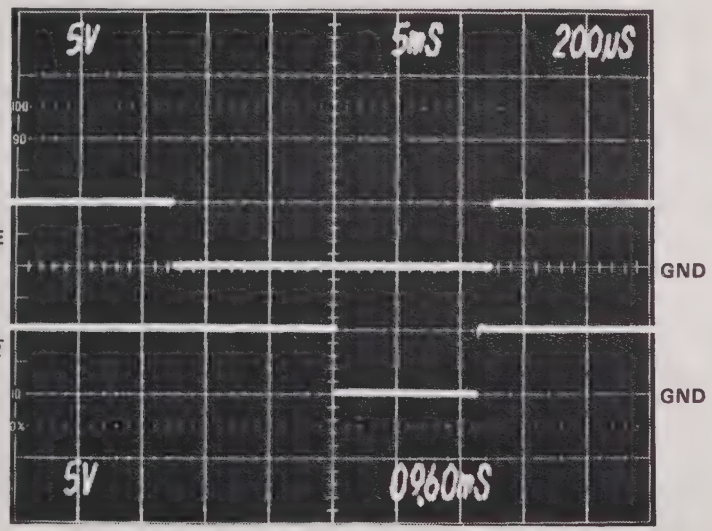
10-950-0059

REVISIONS

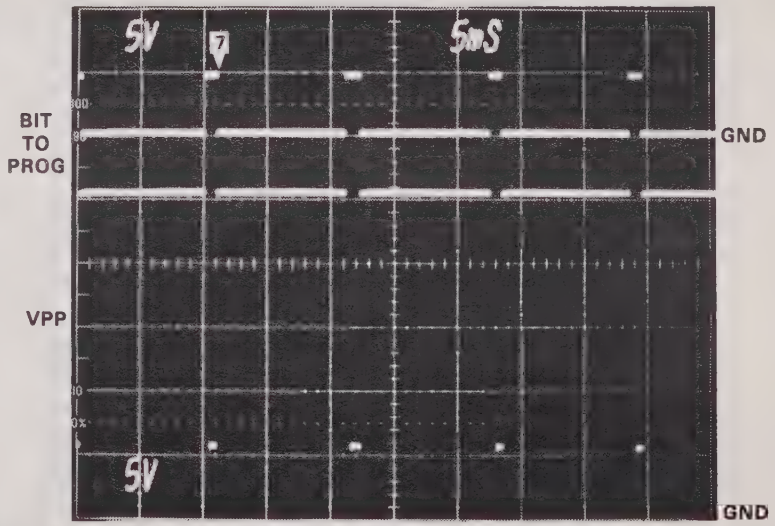
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJJ	11/82
	C	ECN #4831		JH	5/83

DATA I/O ISSAQUAH, WA

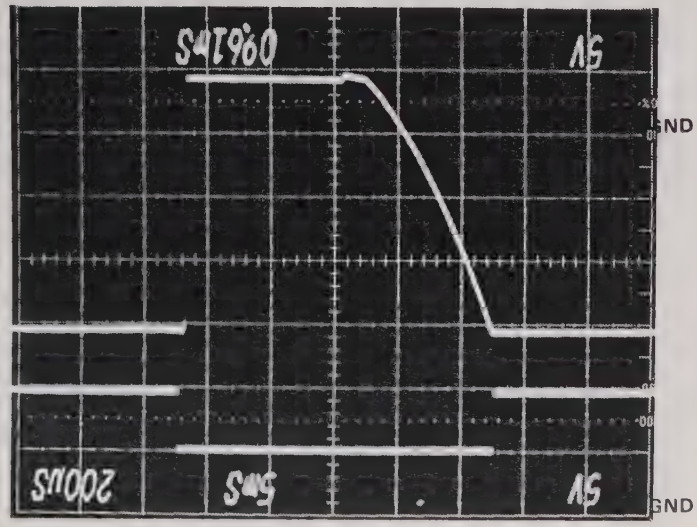
TITLE: TIMING DIAGRAM FAMILY CODES 43, 44	DRAWN BY: EE CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5V
5mS
200uS
PE
GND
E2
GND
5V
0%60mS

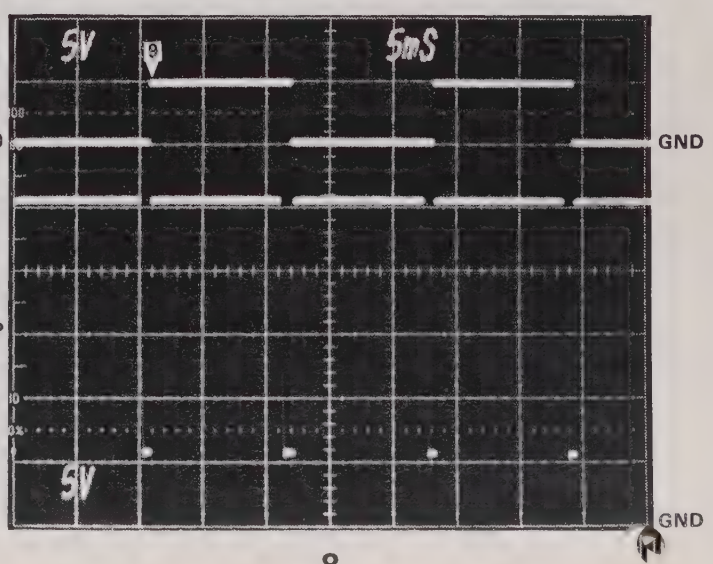
5


5V
7
5mS
BIT
TO
PROG
GND
VPP
5V
GND

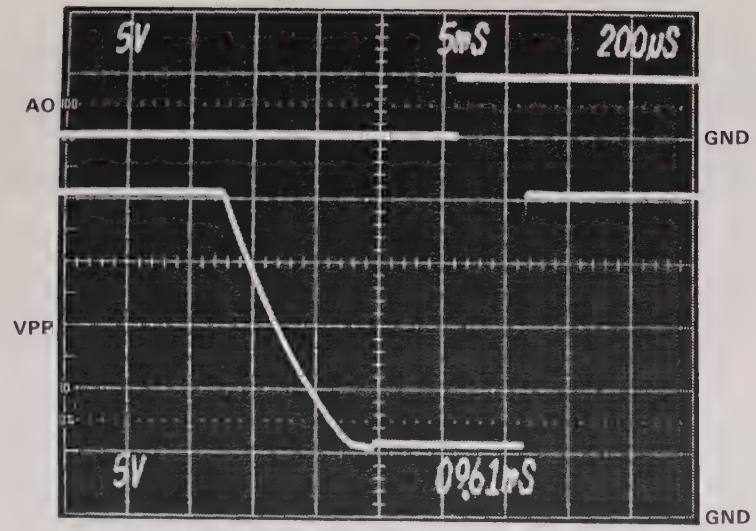
6


BIT
TO
PROG
VPP
GND
GND

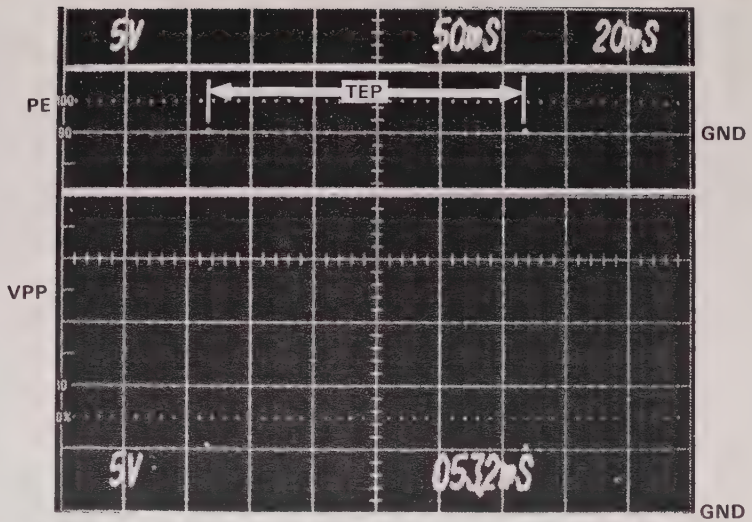
7


5V
8
5mS
A0
GND
VPP
5V
GND

8



9



10

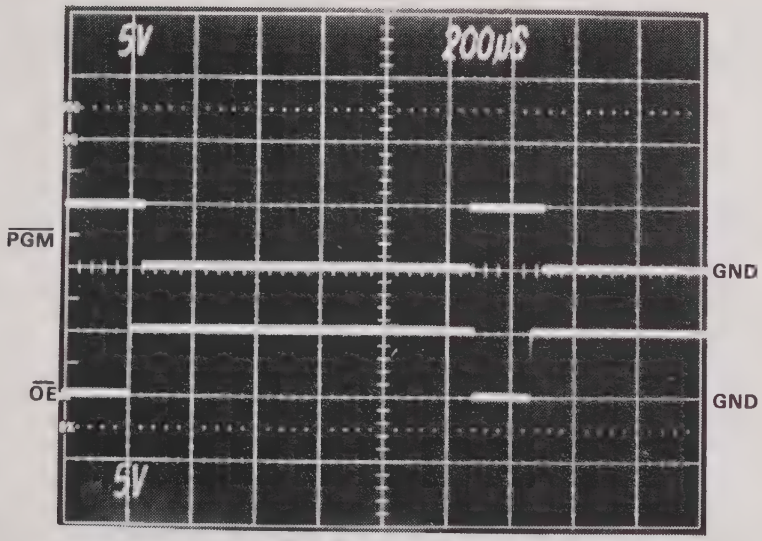
REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		[illegible]	11/82
	C	ECN #4831		[illegible]	[illegible]

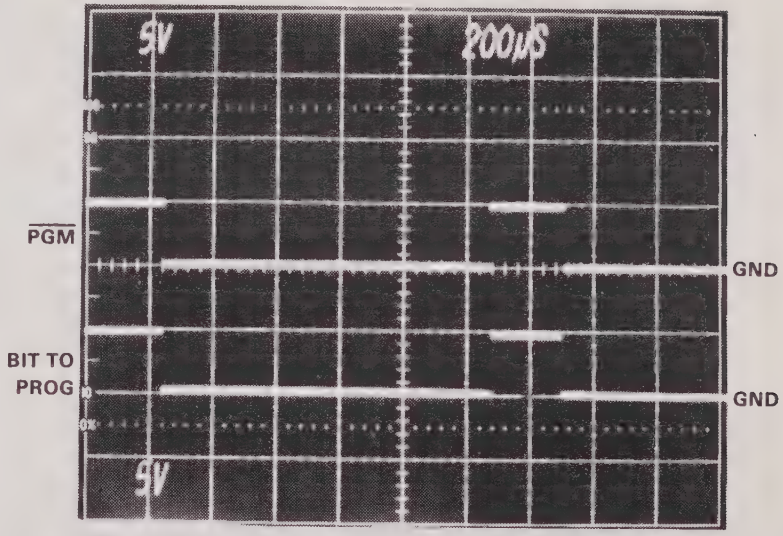
DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM FAMILY CODES 43, 44		DRAWN BY: EE CHECKED BY:
SIZE B	CODE IDENT. NO. 54193	DRAWING NO. 33-950-0059
SCALE		SHEET 2/2

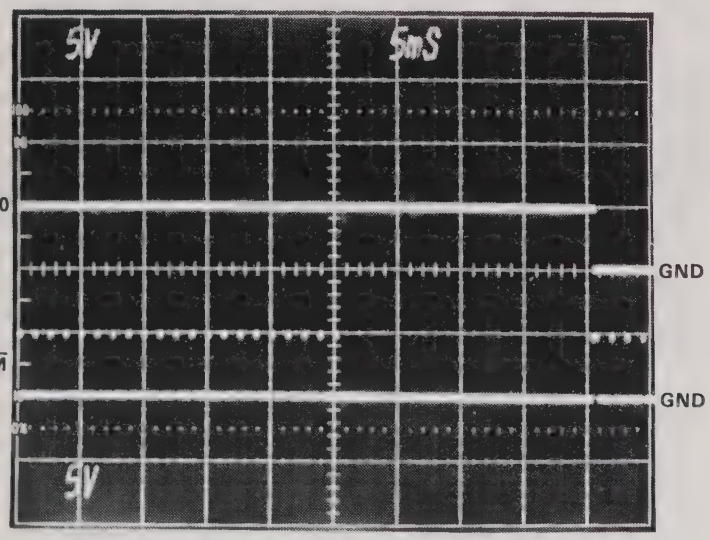
10-950-0059


5V
200μS
PGM
GND
OE
GND
5V

1


5V
200μS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
5mS
A0
GND
PGM
GND
5V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	Not shown
	VPPV					NA
	TPW	.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		20		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 45.*
2. *Load RAM with $01 for Family 46 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 1 ms times the number of programming pulses required to program the location.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		YH	5/85

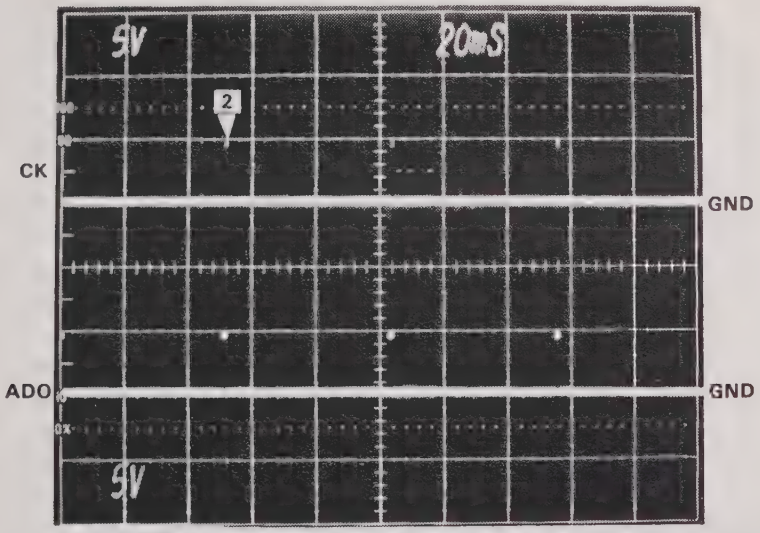
DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODES 45, 46

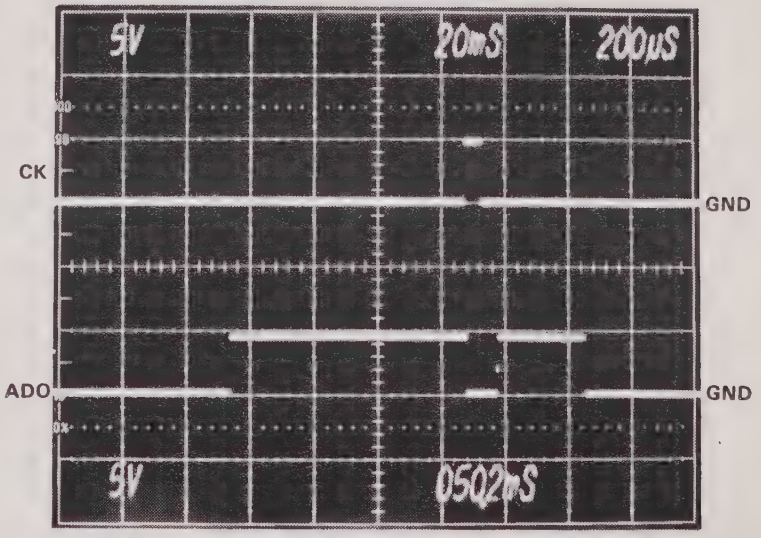
DRAWN BY:

CHECKED BY: YH

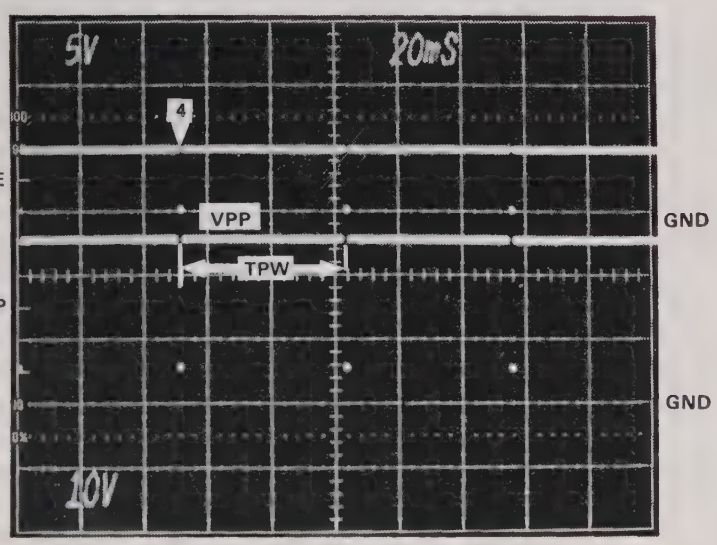
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059


5V
20mS
2
CK
GND
ADO
GND
5V

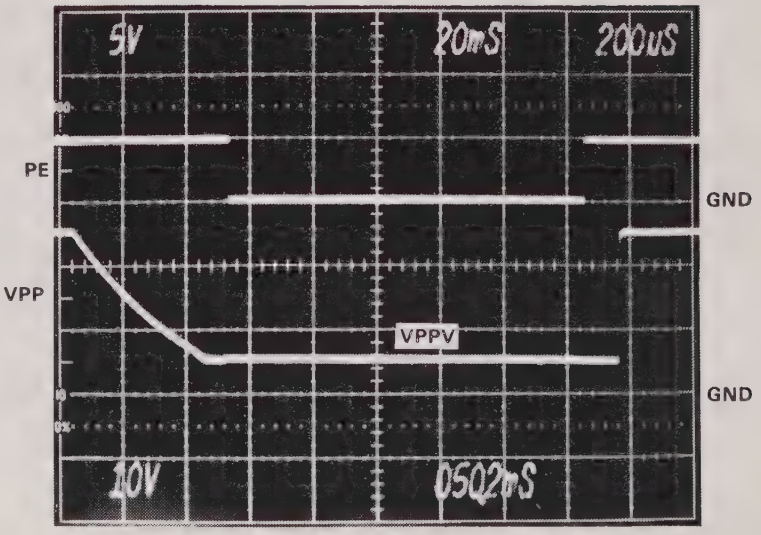
1


5V
20mS
200uS
CK
GND
ADO
GND
5V
0502mS

2


5V
20mS
4
PE
VPP
TPW
GND
VPP
GND
10V

3


5V
20mS
200uS
PE
GND
VPP
VPPV
GND
10V
0502mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not shown
	VOP					NA
	VPP	24.5	25.0	25.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 47.*
2. *Load RAM with $01 for Family 48 and bit-to-prog waveform becomes bit-no-prog waveform.*

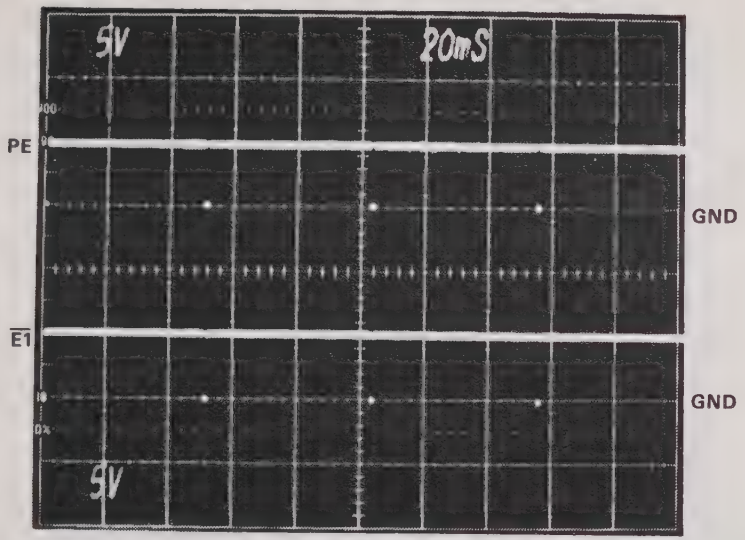
10-950-0059

REVISIONS

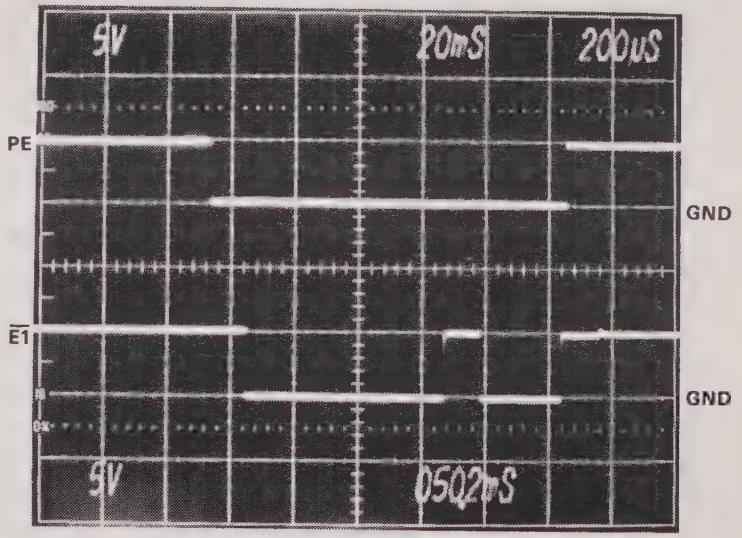
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		XH	5/87

DATA I/O

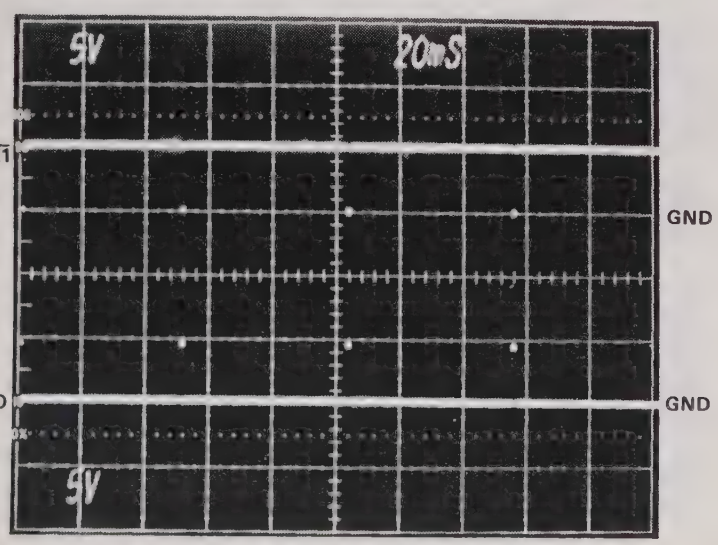
TITLE: TIMING DIAGRAM FAMILY CODES 47, 48		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
20mS
PE
GND
E1
GND
5V

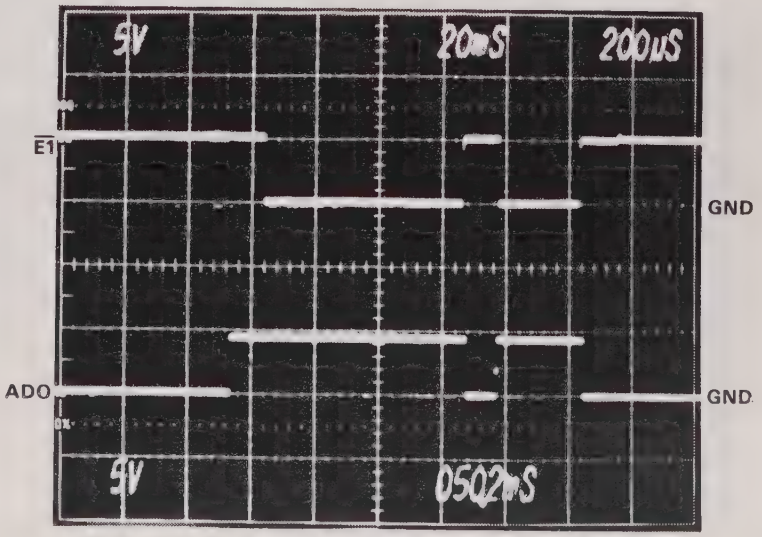
5


5V
20mS
200uS
PE
GND
E1
GND
5V
0502mS

6


5V
20mS
E1
GND
ADO
GND
5V

7


5V
20mS
200uS
E1
GND
ADO
GND
5V
0502mS

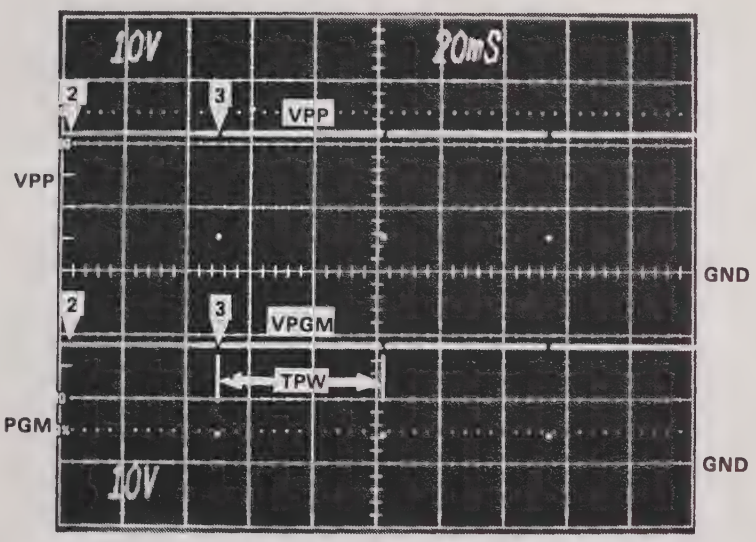
8

10-950-0059

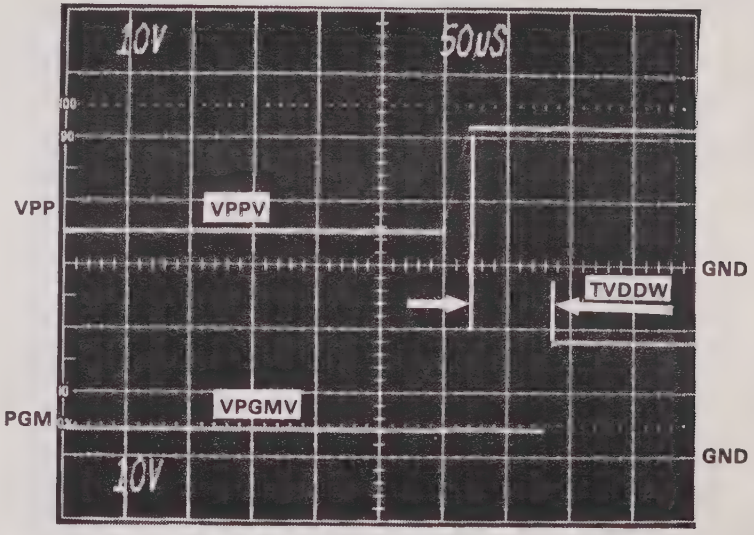
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		LH	4/87

DATA I/O

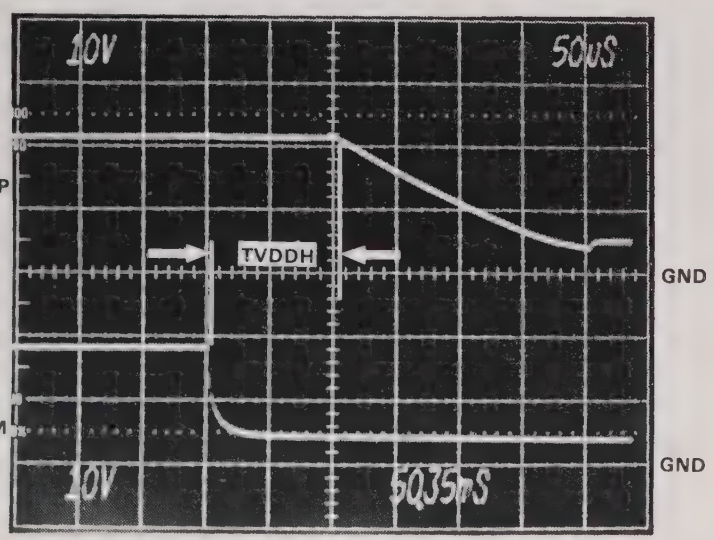
TITLE: TIMING DIAGRAM FAMILY CODES 47, 48		DRAWN BY:
		CHECKED BY: 24
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


10V
20mS
2
3
VPP
VPP
GND
2
3
VPGM
TPW
PGM
GND
10V

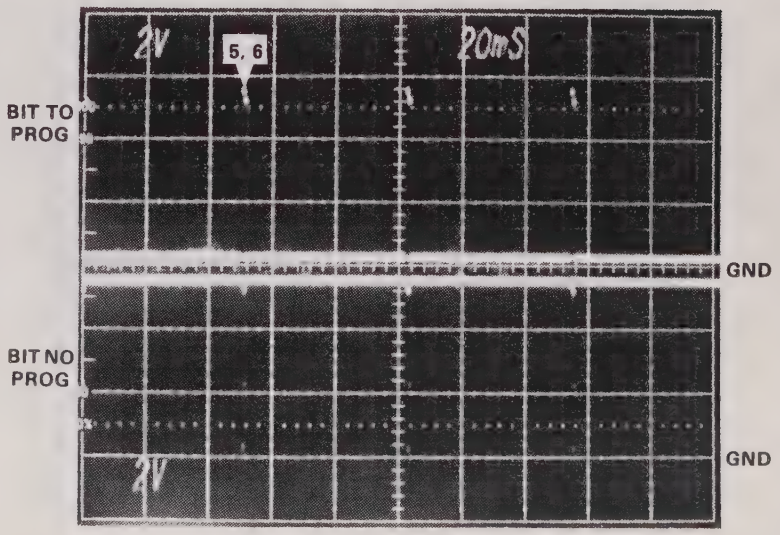
1


10V
50uS
VPP
VPPV
GND
TVDDW
PGM
VPGMV
GND
10V

2


10V
50uS
VPP
TVDDH
GND
PGM
GND
10V
5.035mS

3


2V
5, 6
20mS
BIT TO PROG
GND
BIT NO PROG
GND
2V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	17.5	18.0	18.5	V	Not shown
	VPP	20.5	21.0	21.5	V	
	VPPV	4.8	5.0	5.2	V	
	VPGM	17.5	18.0	18.5	V	
	VPGMV	4.0		5.1	V	
	TVDDW	0		1.0	ms	
	TVDDH	0		1.0	ms	
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 49.*
2. *Load RAM with $01 for Family 50 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17µs @ 3.579545 MHZ*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		CH	[illegible]

DATA I/O

TITLE: TIMING DIAGRAM

FAMILY CODES 49, 50

DRAWN BY:

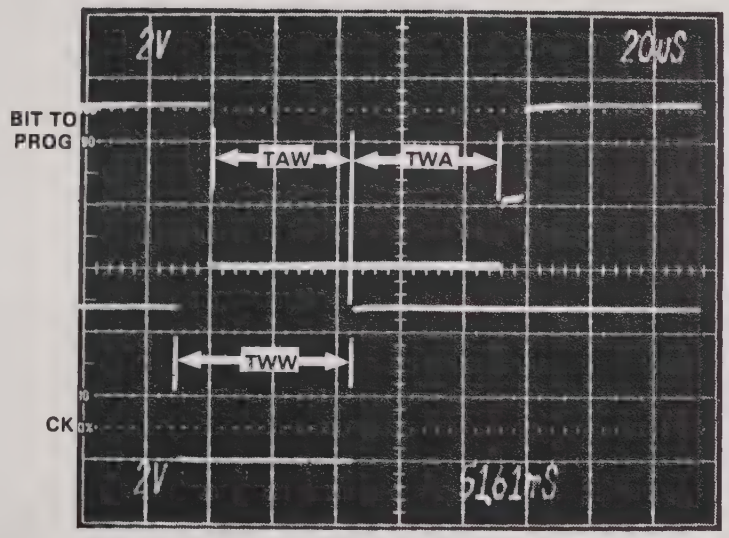
CHECKED BY: CH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

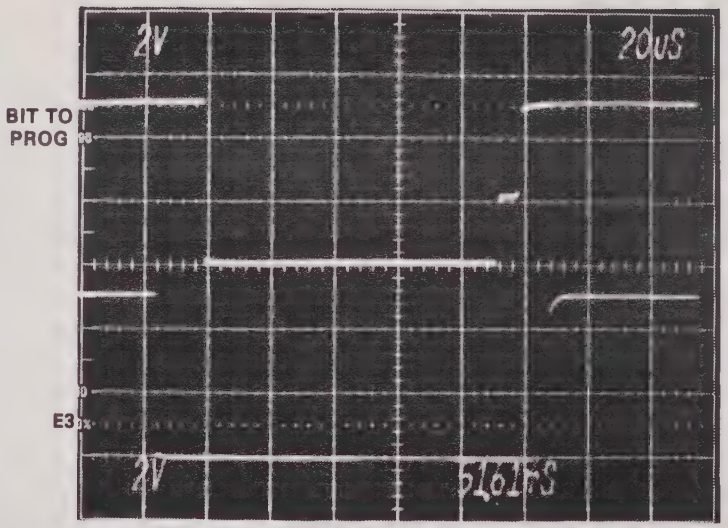
SCALE

SHEET 1 of 2

10-950-0059


2V
20uS
BIT TO PROG
TAW
TWA
TWW
CK
2V
5161-5

5


2V
20uS
BIT TO PROG
E3
2V
5161-5

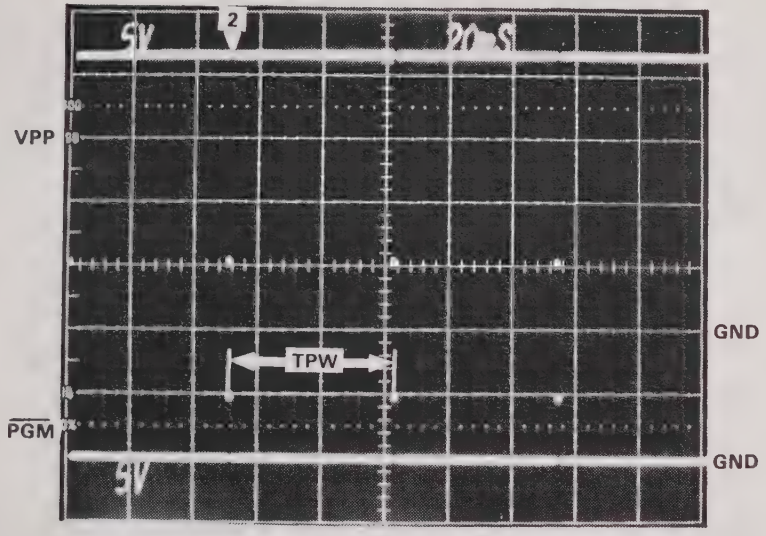
6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831			

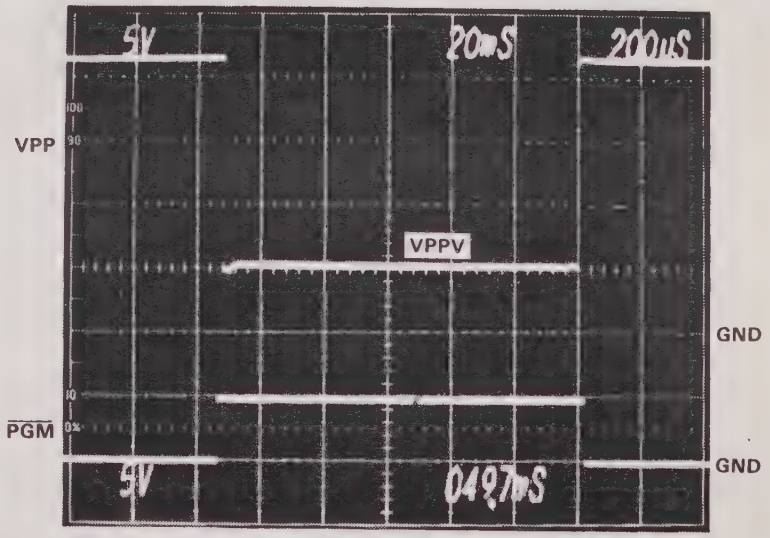
DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES 49, 50		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2

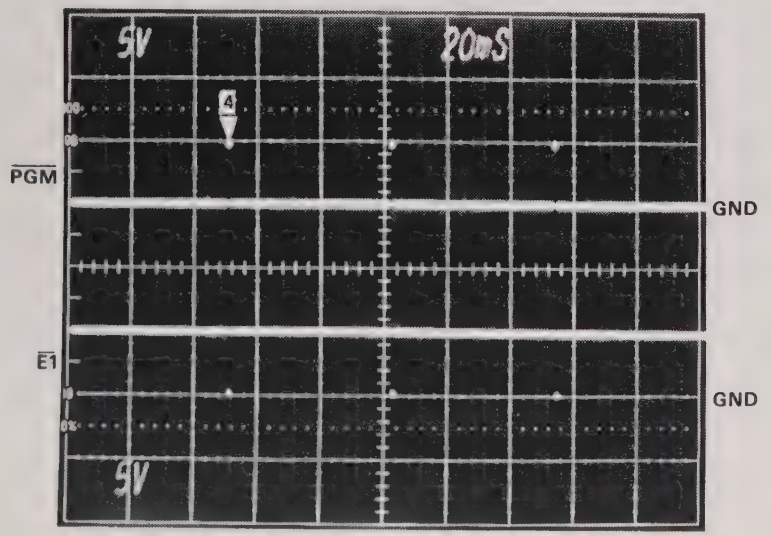
10-950-0059


5V
2
20mS
VPP
TPW
GND
PGM
GND
5V

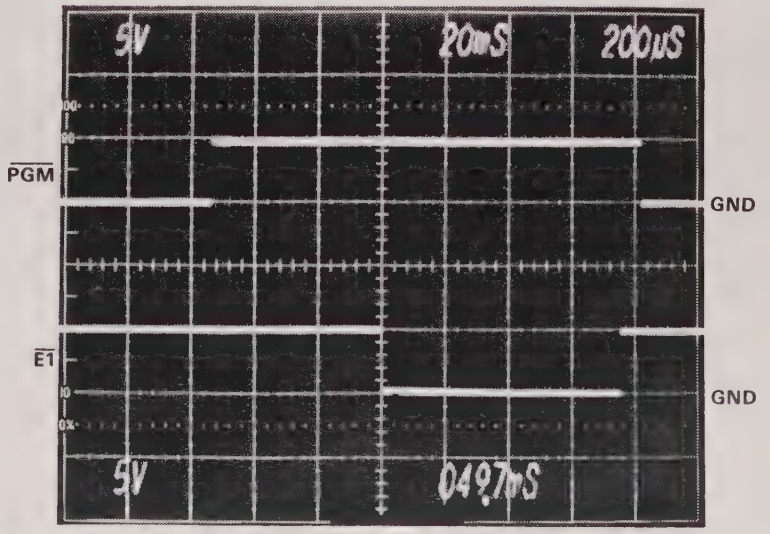
1


5V
20mS
200µS
VPP
VPPV
GND
PGM
GND
5V
049.7mS

2


5V
20mS
4
PGM
GND
E1
GND
5V

3


5V
20mS
200µS
PGM
GND
E1
GND
5V
049.7mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 53.*
2. *Load RAM with $01 for Family 54 and bit-to-prog waveform becomes bit-no-prog waveform.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831			

DATA I/O

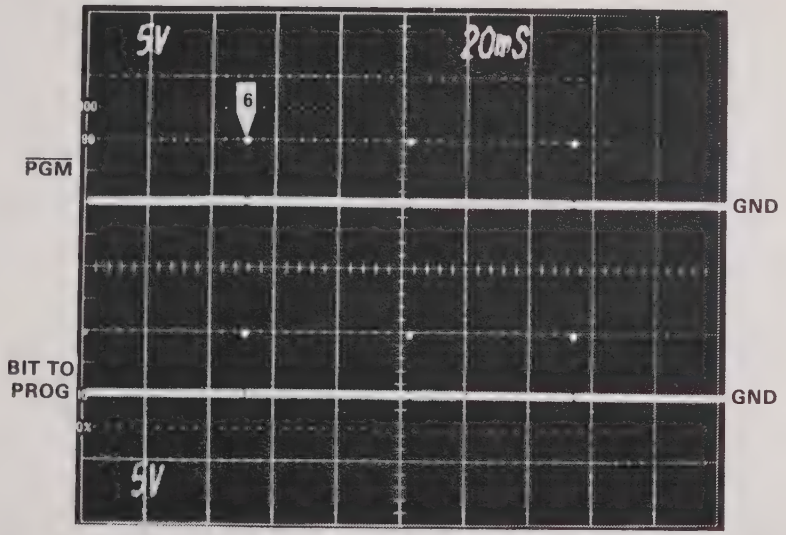
TITLE: TIMING DIAGRAM — FAMILY CODES 53, 54

DRAWN BY:

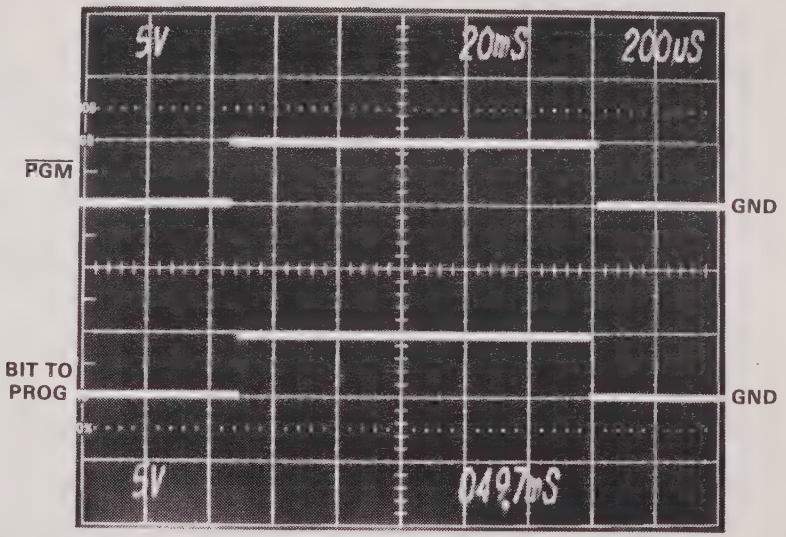
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

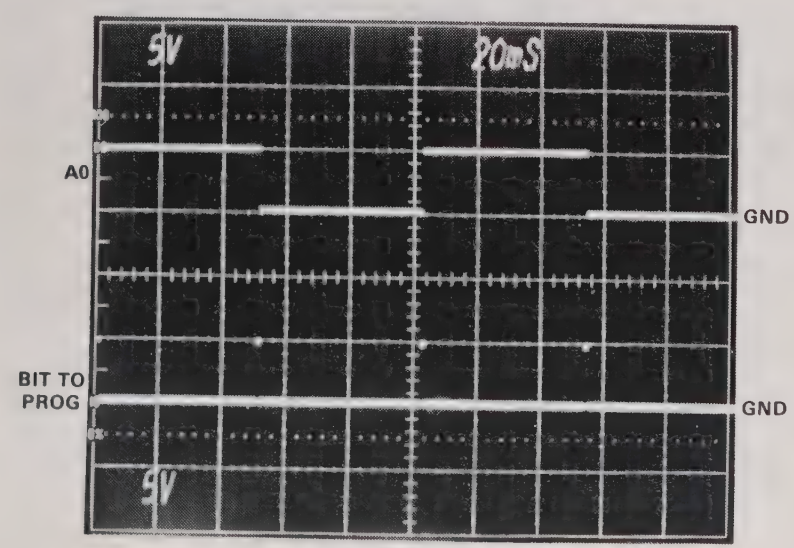
SCALE


5V
20mS
6
PGM
GND
BIT TO
PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO
PROG
GND
5V
049.7mS

7


5V
20mS
A0
GND
BIT TO
PROG
GND
5V

6

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		KM	5/83

DATA I/O

TITLE

TIMING DIAGRAM

FAMILY CODES 53, 54

DRAWN BY:

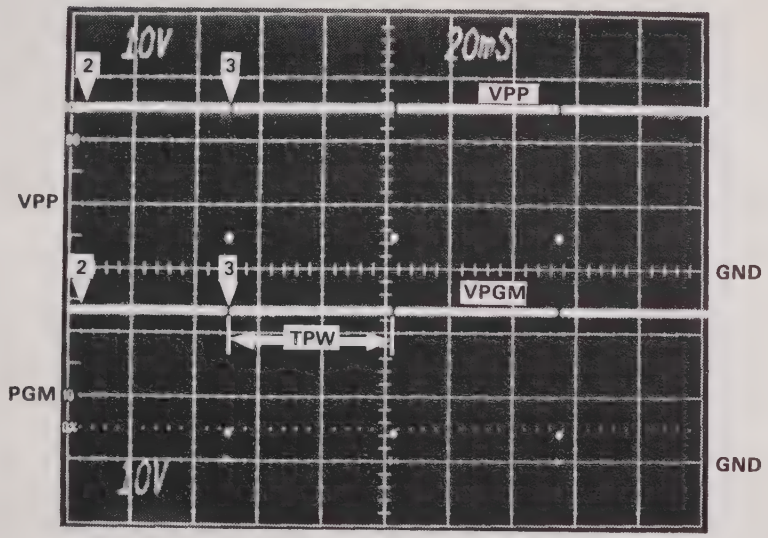
CHECKED BY: KH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

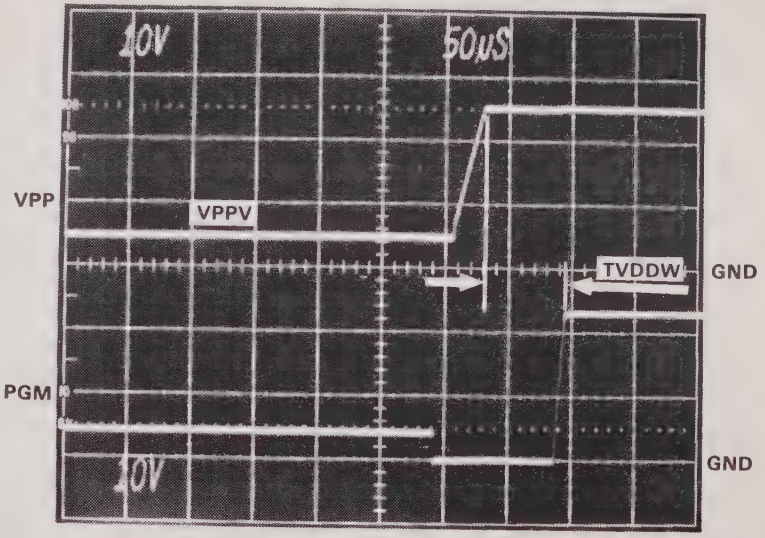
SCALE

SHEET 2 of 2

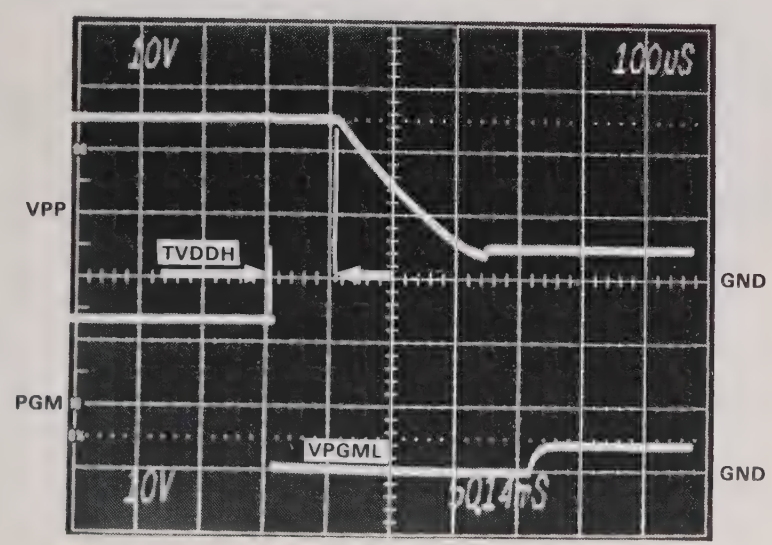
10-950-0059


10V
20mS
2
3
VPP
VPP
2
3
GND
VPGM
TPW
PGM
10V
GND

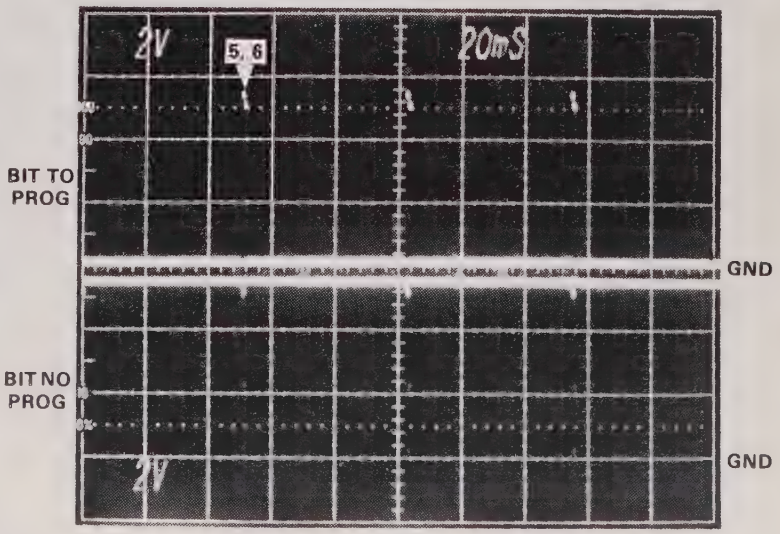
1


10V
50uS
VPP
VPPV
TVDDW
GND
PGM
10V
GND

2


10V
100uS
VPP
TVDDH
GND
PGM
VPGML
10V
GND

3


2V
5, 6
20mS
BIT TO PROG
GND
BIT NO PROG
2V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	21.5	23.0	24.5	V	Not shown
	VPP	24.0	25.0	26.0	V	
	VPPV	4.0	5.0	5.2	V	
	VPGM	21.5	23.0	24.5	V	
	VPGML		0	0.3	V	
	TVDDW	17			µs	See note 3
	TVDDH	0			µs	See note 3
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 55.*
2. *Load RAM with $01 for Family 56 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17 µs @ 3.579545 MHZ*

10-950-0059

REVISIONS

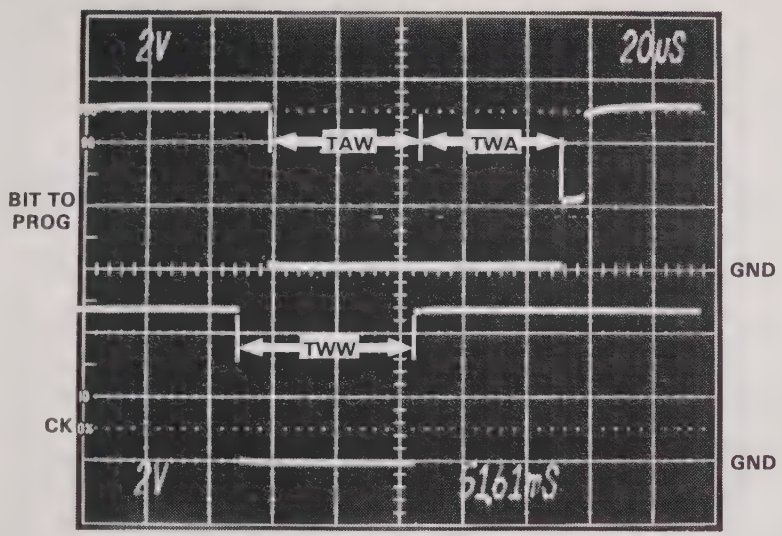
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XH	5/83

DATA I/O

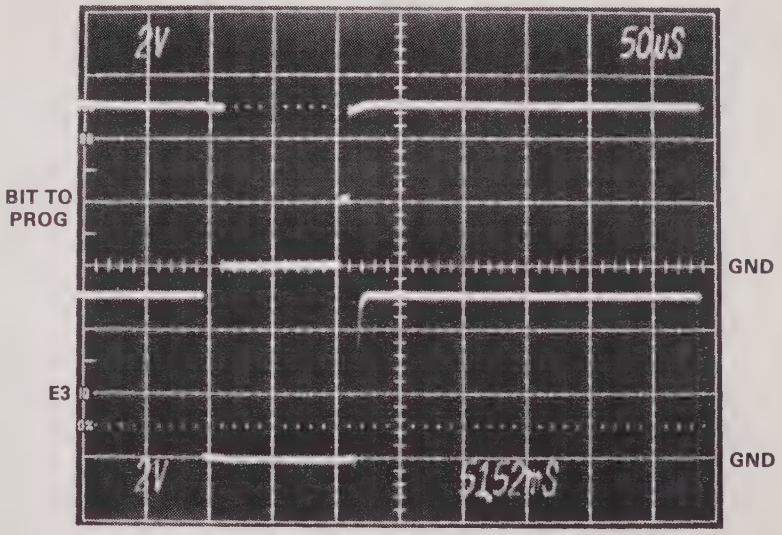
TITLE: TIMING DIAGRAM FAMILY CODES 55, 56	DRAWN BY:
	CHECKED BY: XH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 1 of 2



5



6

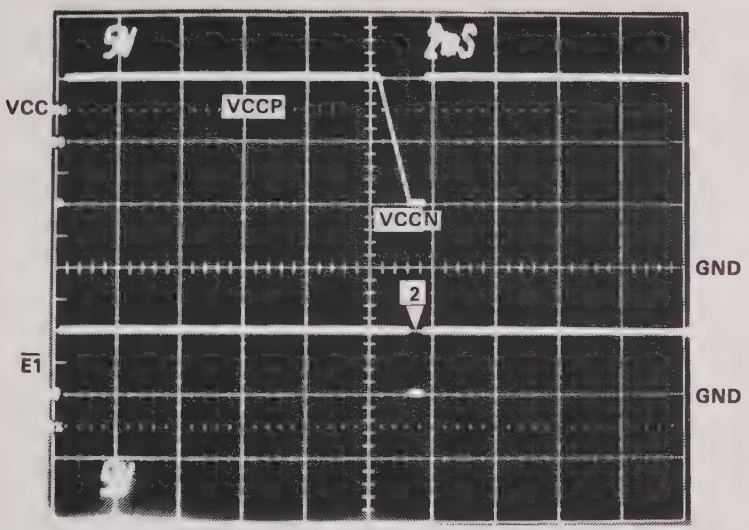
10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XA	5/83

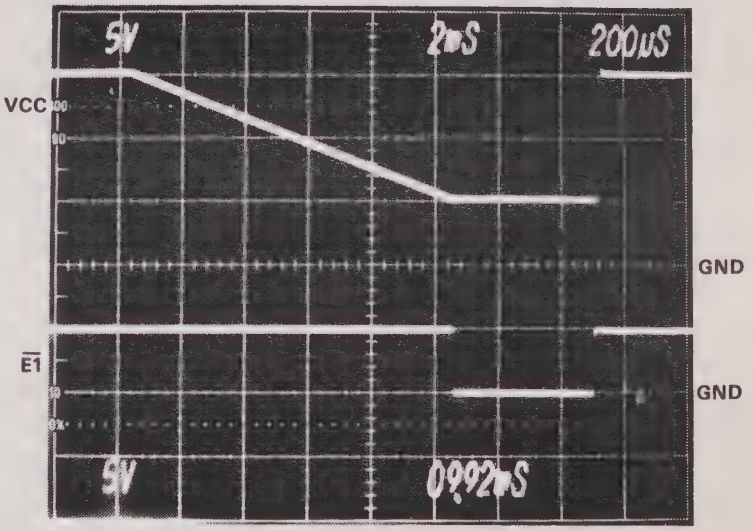
DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES 55, 56		DRAWN BY:
		CHECKED BY: XA
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2

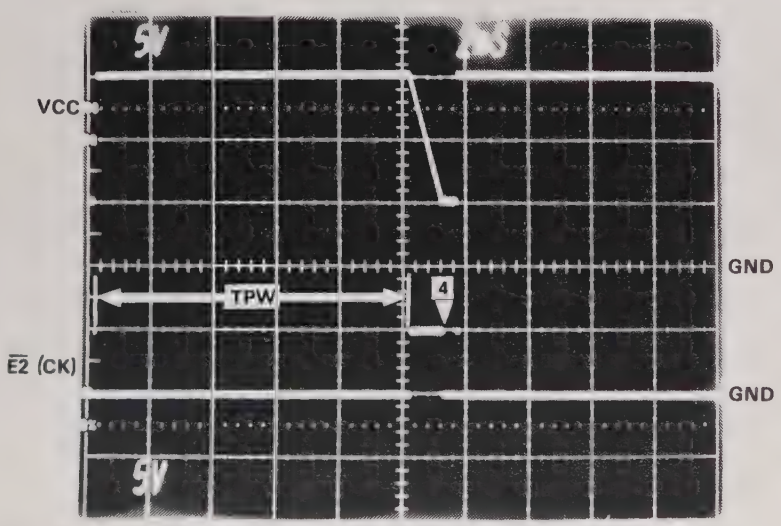
10-950-0059


5V
2mS
VCC
VCCP
VCCN
GND
2
E1
GND
5V

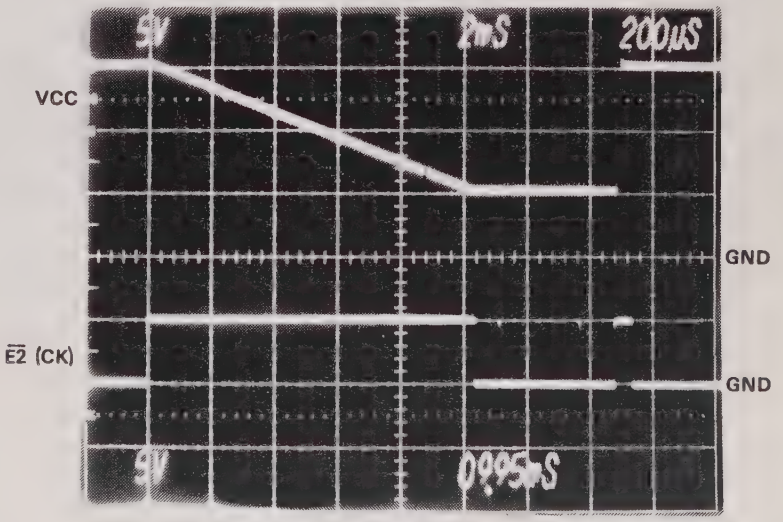
1


5V
2mS
200µS
VCC
GND
E1
GND
5V
0.92mS

2


5V
VCC
GND
TPW
4
E2 (CK)
GND
5V

3


5V
2mS
200µS
VCC
GND
E2 (CK)
GND
5V
0.95mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	14.0	15.0	16.0	V	
	VCCN	4.0	5.0	6.0	V	
	TPW	9.8	10.0	10.2	ms	
	TR					NA
	TF					NA
	Reject		2		Pulse	
	Overprogram		0		Pulse	
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 57, and Bit-no-Prog waveform becomes Bit-to-Prog waveform.*
2. *Load RAM with $01 for Family 58.*
3. *Photos 7 and 8 are erase waveforms*
4. *On the E2(CK) pin, one or two clock pulses may be seen depending on which pulse location is observed.*
5. *Photo 5 is for Family 58. For Family 57 it is Bit-to-Prog.*

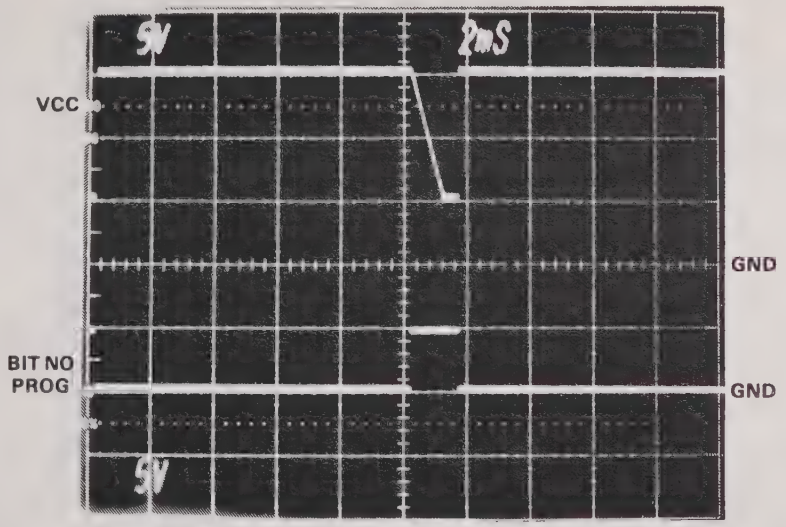
10-950-0059

REVISIONS

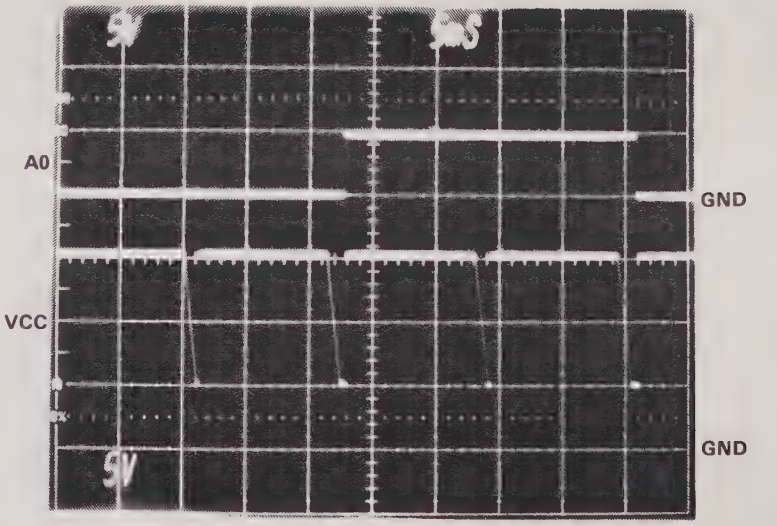
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XH	2/23

DATA I/O

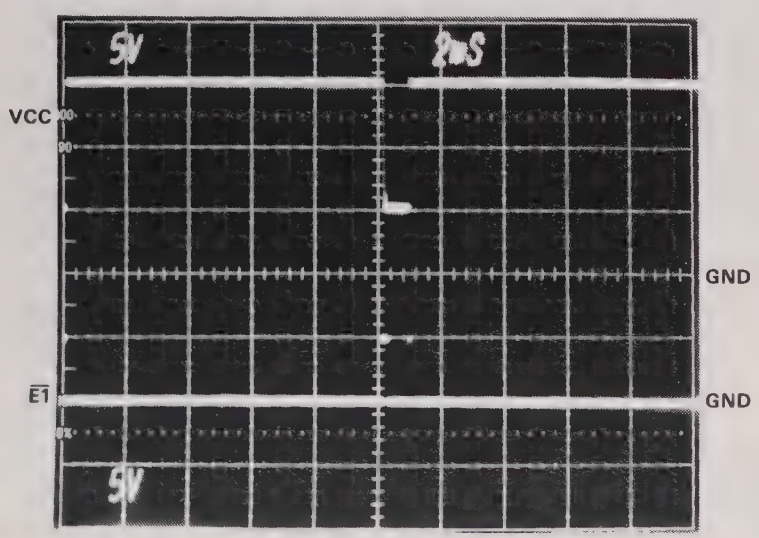
TITLE: TIMING DIAGRAM FAMILY CODES 57, 58	DRAWN BY:	CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
2mS
VCC
GND
BIT NO
PROG
GND
5V

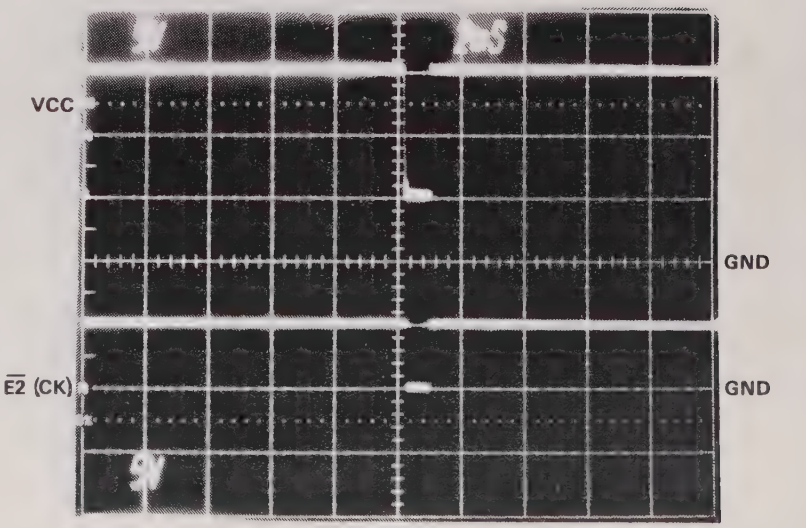
5


5V
2mS
A0
GND
VCC
GND
5V

6


5V
2mS
VCC
GND
$\overline{E1}$
GND
5V

7


5V
2mS
VCC
GND
$\overline{E2}$ (CK)
GND
5V

8

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831			

DATA I/O

TITLE

TIMING DIAGRAM

FAMILY CODES 57, 58

DRAWN BY:

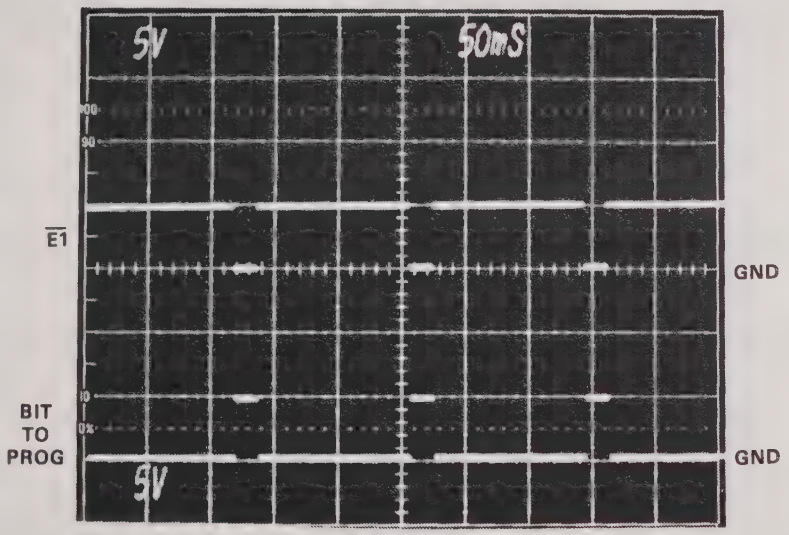
CHECKED BY: XH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

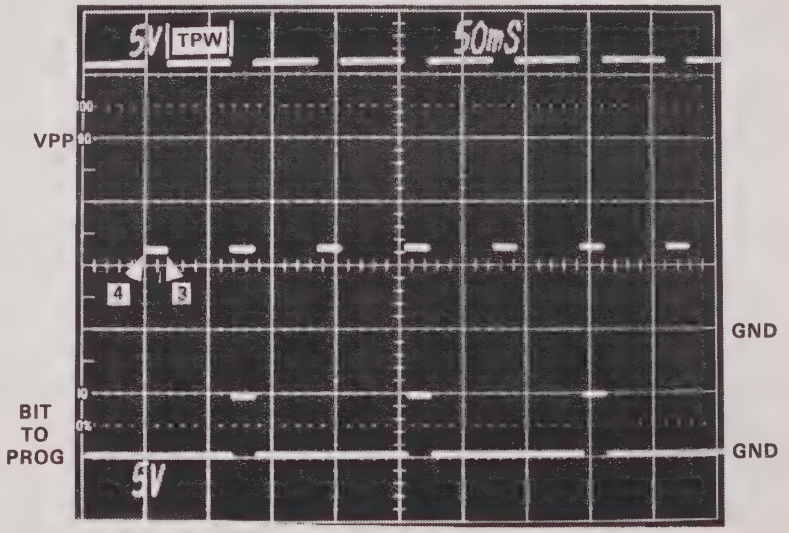
SCALE

SHEET 2 of 2

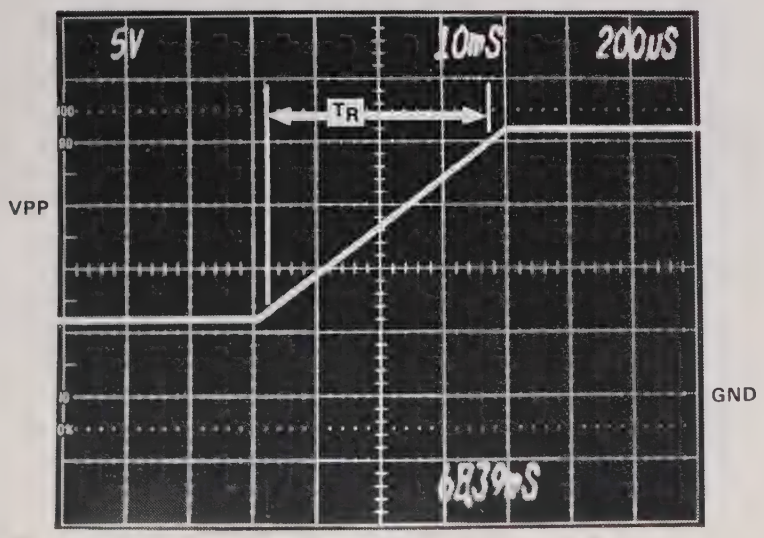
10-950-0059



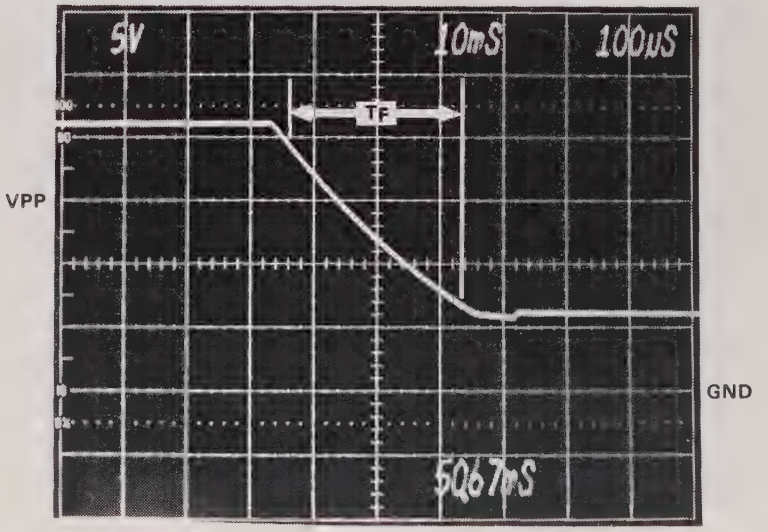
1



2



3



4

10-950-0056

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.5	5.8	6.1	V	Not Shown
	VPP	20.0	20.5	21.0	V	
	VPPN	5.7	5.9	6.1	V	
	TPW	45	50	55	ms	
	T_R	50			µs	
	T_F	50			µs	
	Reject		4		Pulses	See note 3
	Overprogram		1		Pulses	See note 3
1ST PASS VERIFY	VCC	4.8	4.9	5.0	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	16.4	17.4	18.4	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	19.1	20.1	21.1	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 59.*
2. *Load RAM with $01 for Family 60, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *Pulse 2 of the 4 pulse string is actually an overprogram pulse.*

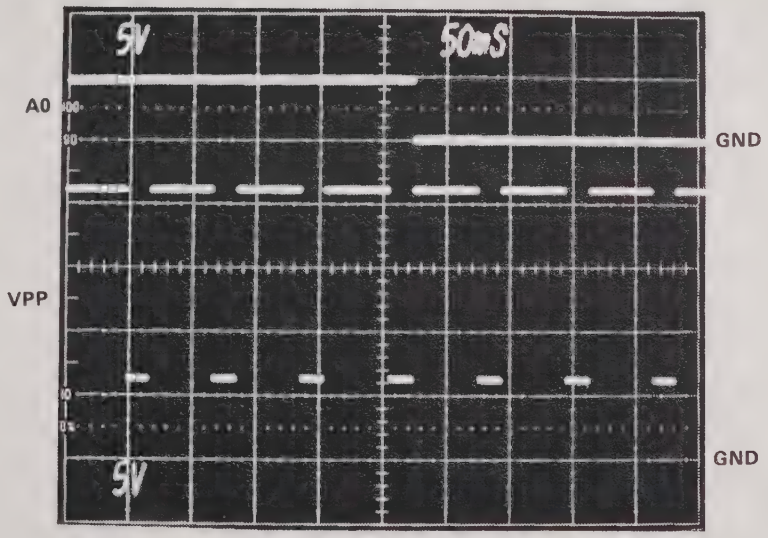
10-960-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		XP	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 59, 60	DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1/2



5

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		[illegible]	11/82
	C	ECN #4831		[illegible]	[illegible]

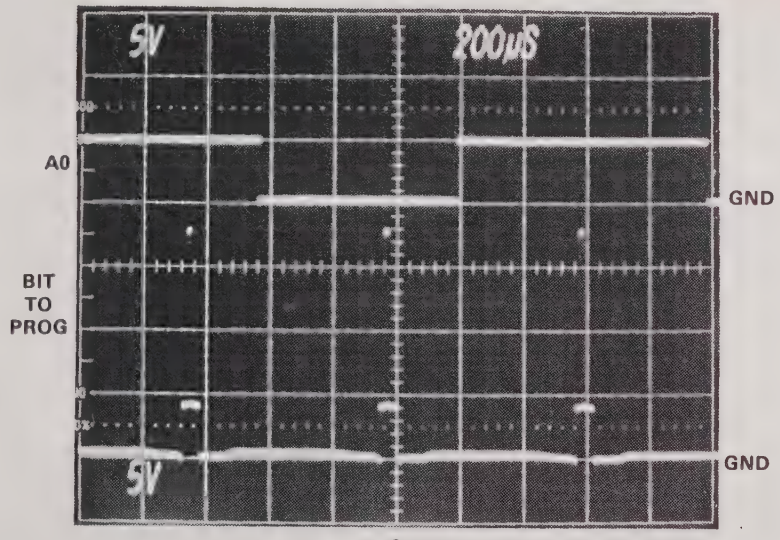
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 59, 60	DRAWN BY: CHECKED BY:

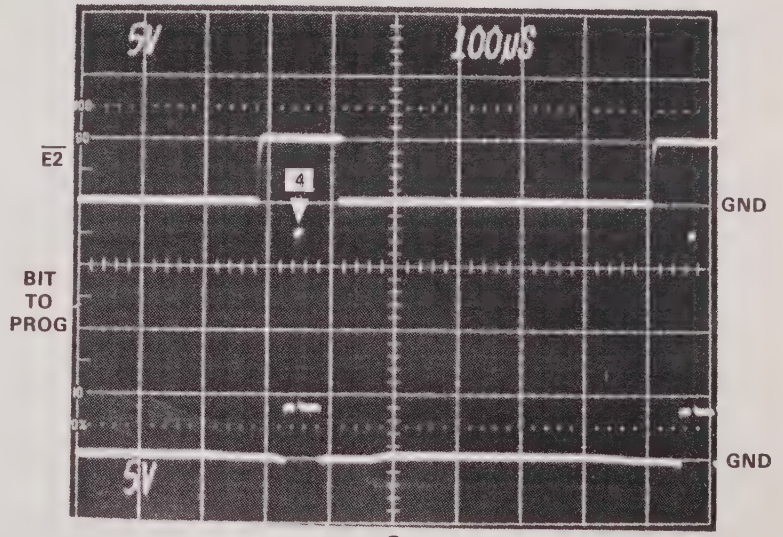
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 2/2

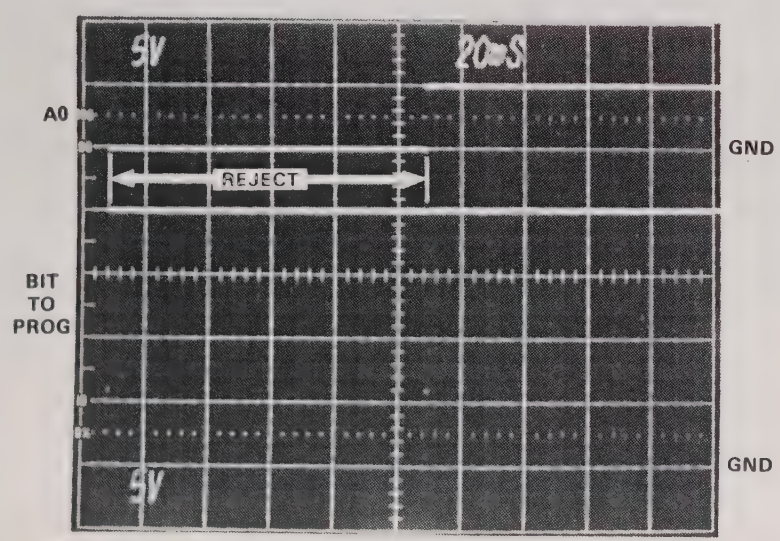
10-950-0059



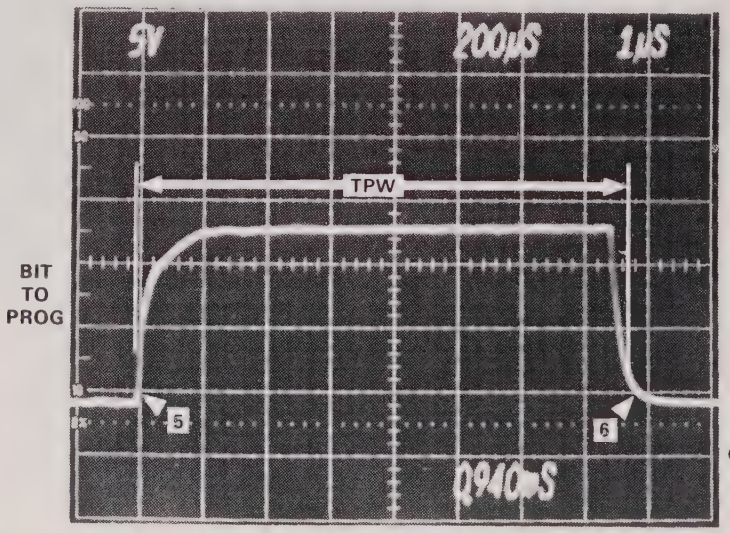
1



2



3



4

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VOP	19.0	19.5	20.0	V	
	TPW	7.1	7.5	7.9	µs	See Note 2
	TR	.16		1.1	µs	
	TF	.16		1.1	µs	
	Overprogram		1		Pulses	
	Reject		10000		Pulses	See Note 3
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.5	4.6	4.7	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.5	6.6	6.7	V	
	VREF	4.4	4.5	4.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.7	7.2	7.7	V	701-1655/TP3

NOTES

1A. Fill RAM with $FE for Family 65.
1B. Fill RAM with $01 for Family 66.
2. Measurement taken at 9V point of 01 with a 200Ω load.
3. 10,000 pulses equals 100ms as shown in photo number 3.
4. Do not use a wirewound load resistor.
5. For pinouts 16 and 21, $\overline{E2}$ is seen on $\overline{E1}$.

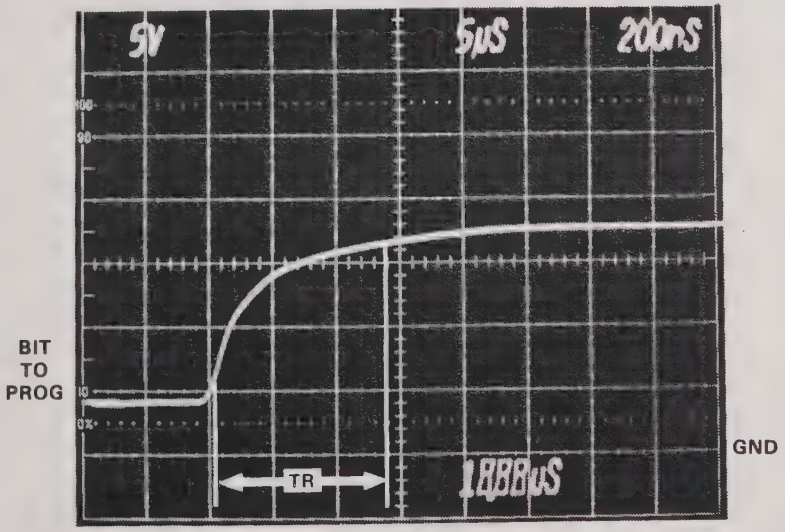
10-950-0059

REVISIONS

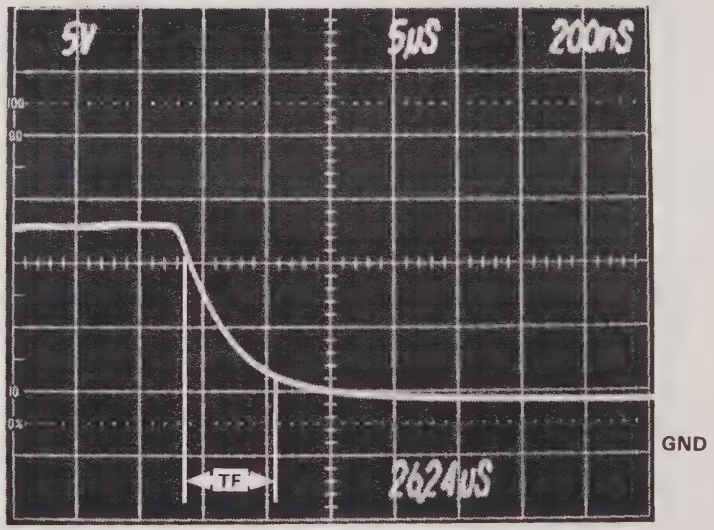
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		24	5/3

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 65, 66	DRAWN BY: PAP
	CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1/2


5V
5µS
200nS
BIT
TO
PROG
GND
TR
188µS

5


5V
5µS
200nS
GND
TF
2624µS

6

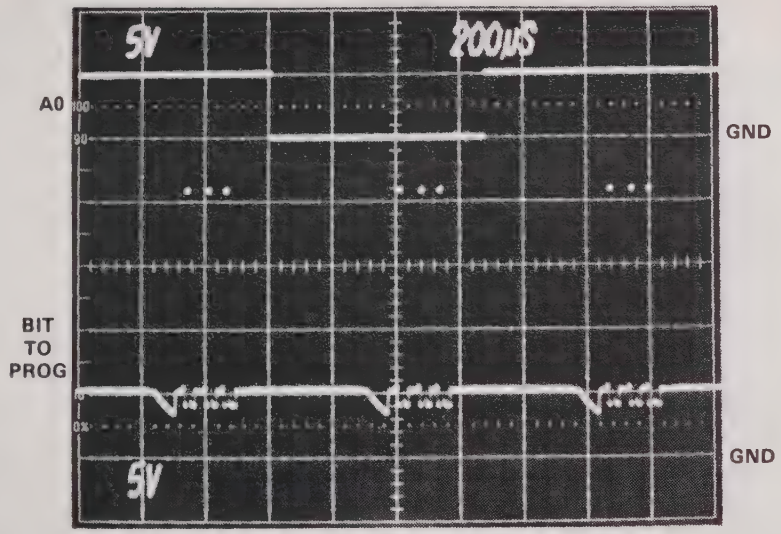
REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XH	5/8

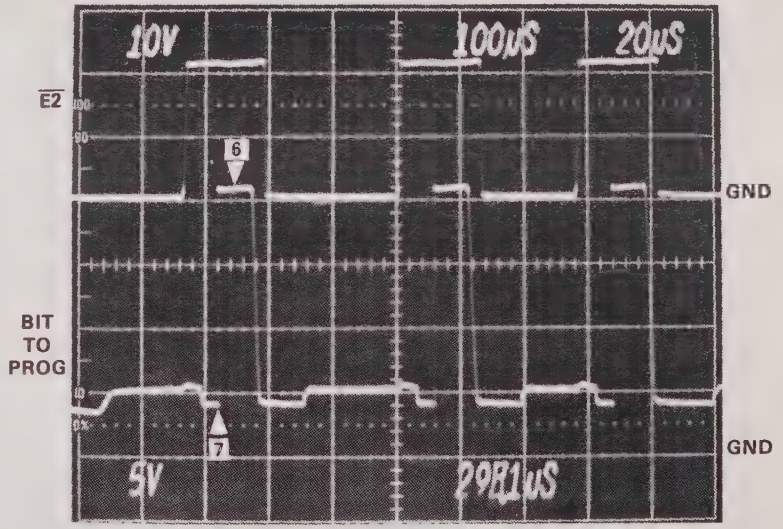
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 65, 66	DRAWN BY: PAP	
	CHECKED BY: XH	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

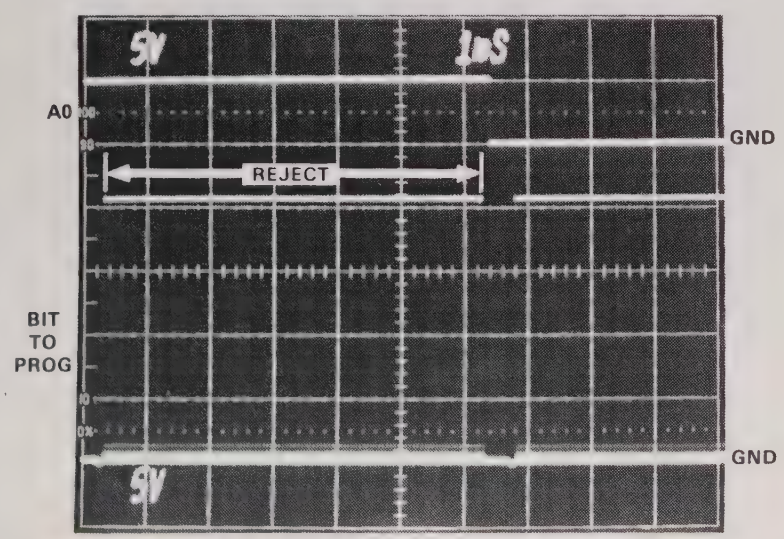
10-950-0059


5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

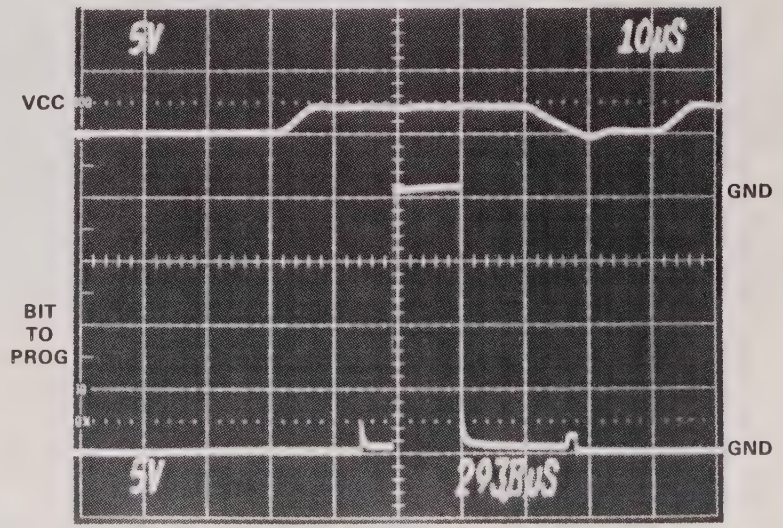
1


10V
100µS
20µS
E2
6
GND
BIT
TO
PROG
7
GND
5V
29R1µS

2


5V
1µS
A0
GND
REJECT
BIT
TO
PROG
GND
5V

3


5V
10µS
VCC
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	6.7	7.0	7.5	V	
	VPP	20.0	20.0	22.0	V	
	VOP	20.0	20.0	22.0	V	
	TPW	10.0	11.0	12.0	µs	See Note 2
	TR			2.0	µs	
	TF			2.0	µs	
	Overprogram		2		Pulses	
	Reject		100		Pulses	See Note 3
	Duty Cycle	15	20	25	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.9	7.0	7.1	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	5.6	6.6	7.6	V	701-1655/TP3

NOTES

1A. Fill RAM with $FE for Family 67.
1B. Fill RAM with $01 for Family 68.
2. Measurement taken at 15V point of 01 with a 200Ω load.
3. 100 pulses equals 6ms as shown in photo number 3.
4. VCC loaded with a 330Ω resistor as shown in photo 5.
5. Do not use a wirewound load resistor.
6. 01 is loaded with a 200Ω resistor in photos 3-7.

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.	11/82
	C	ECN #4831			5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 67, 68

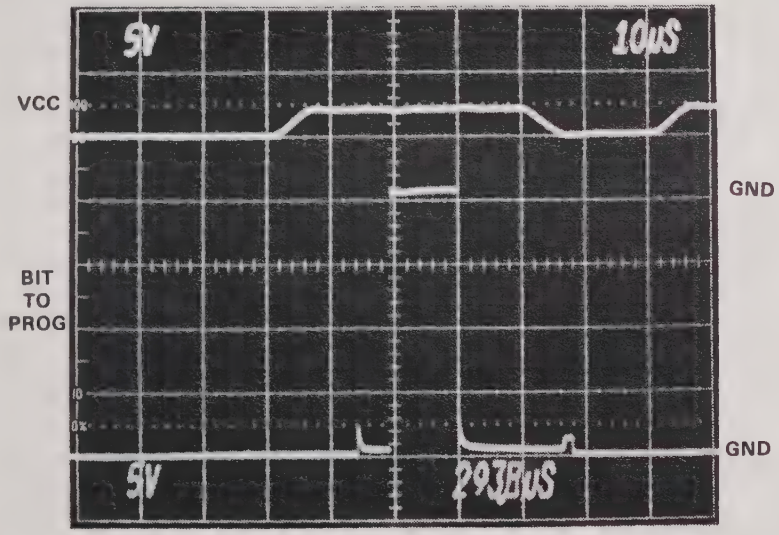
DRAWN BY: BG / PP

CHECKED BY:

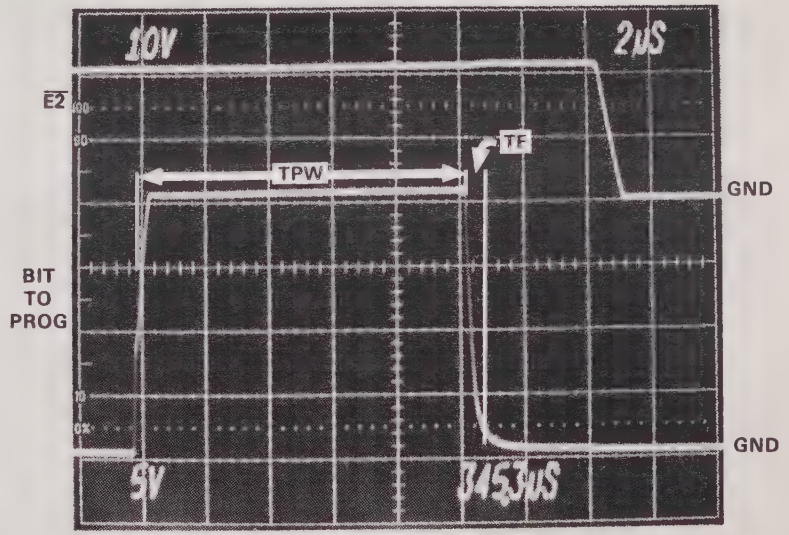
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

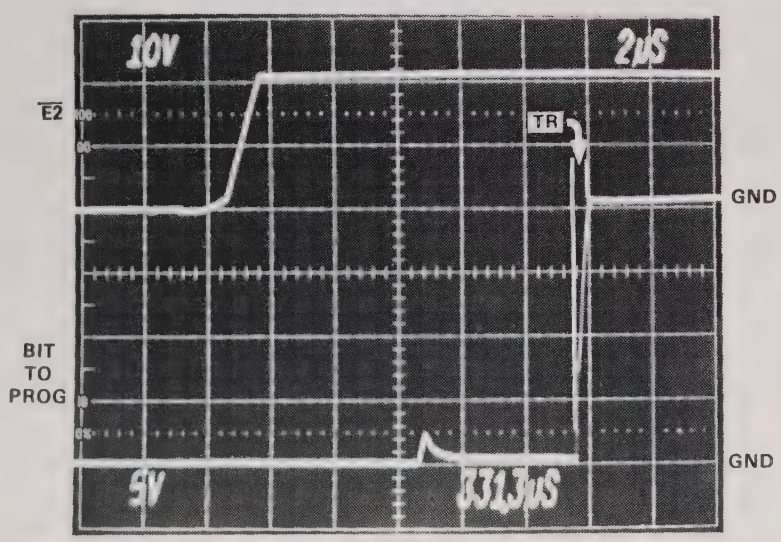
SHEET 1/2


5V
10µS
VCC
GND
BIT
TO
PROG
GND
5V
2938µS

5


10V
2µS
E2
TF
TPW
GND
BIT
TO
PROG
GND
5V
3453µS

6


10V
2µS
E2
TR
GND
BIT
TO
PROG
GND
5V
1313µS

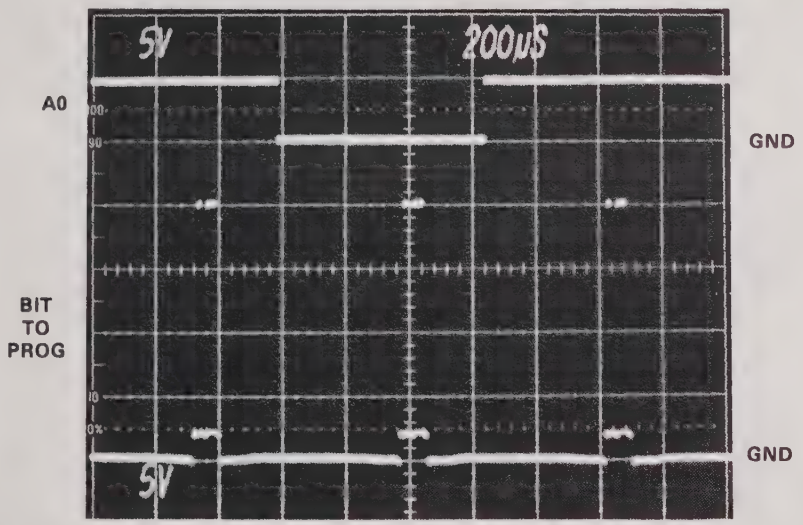
7

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		XH	5/83

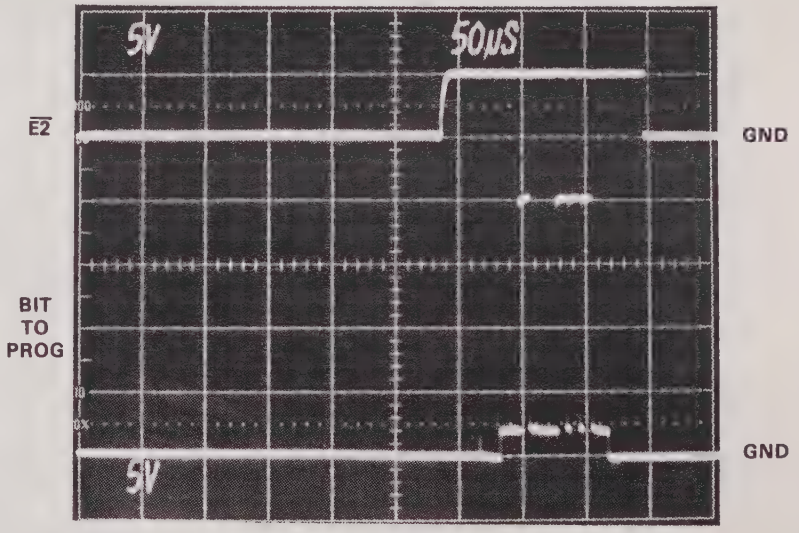
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 67, 68		DRAWN BY: BG / PAP CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

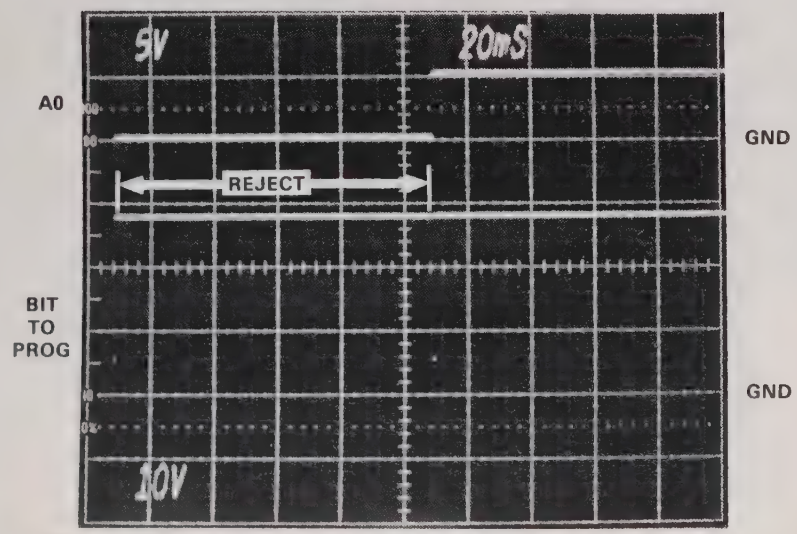
10-960-0059



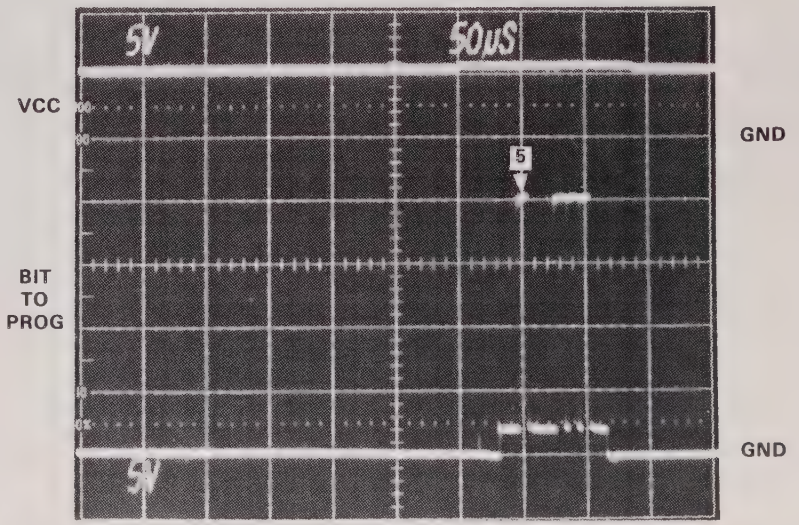
1



2



3



4

10-920-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	µs	See Note 2
	T_R	0.21		0.30	µs	
	T_F	0.21		0.30	µs	
	Overprogram		4		Pulses	
	Reject		10000		Pulses	See Note 3
	Duty Cycle	70	75	80	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	6.9	7.0	7.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.6	9.6	10.6	V	701-1655/TP3

NOTES

1A. Fill RAM with $FE for Family 69.
1B. Fill RAM with $01 for Family 70.
2. Measurement taken at 10V point of 01 with a 100Ω load.
3. 10,000 pulses equals 100ms as shown in photo number 3.
4. Do not use a wirewound load resistor.

10-950-0059

REVISIONS

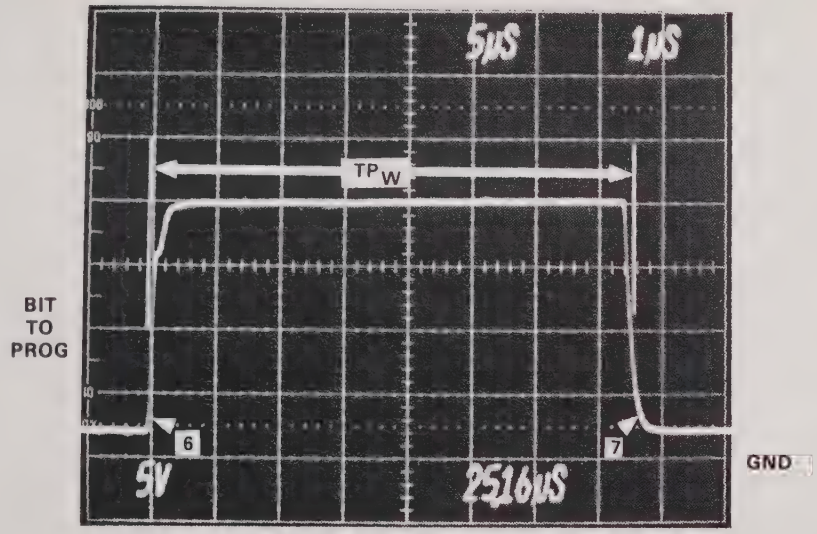
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.B.	11/82
	C	ECN #4831		[illegible]	[illegible]

DATA I/O ISSAQUAH, WA

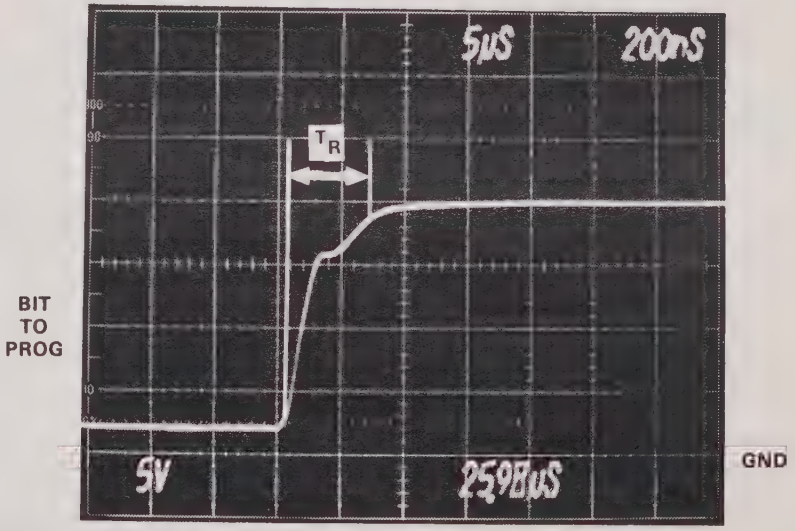
TITLE: TIMING DIAGRAM	DRAWN BY:
FAMILY CODES 69, 70	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

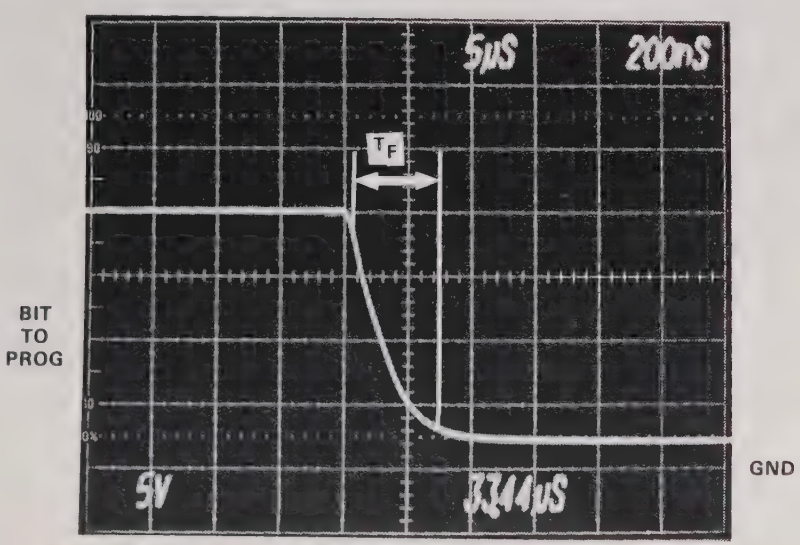
SCALE | SHEET 1/2



5



6



7

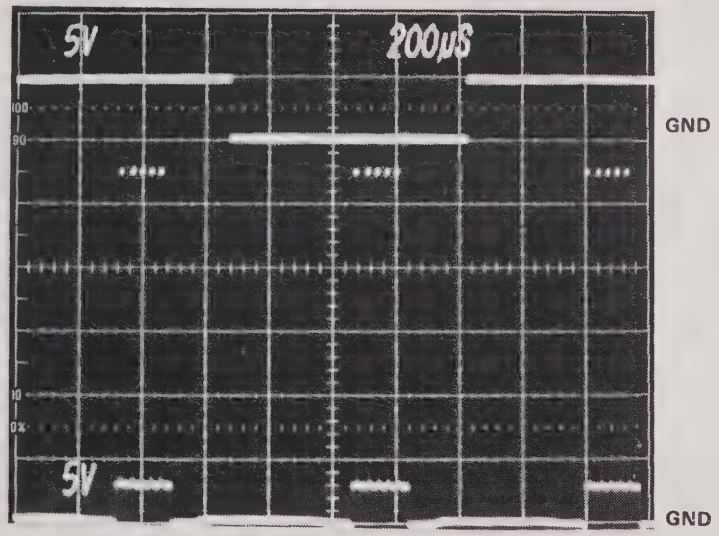
10-960-0069

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.I.3.	11/82
	C	ECN #4831		XA	5/83

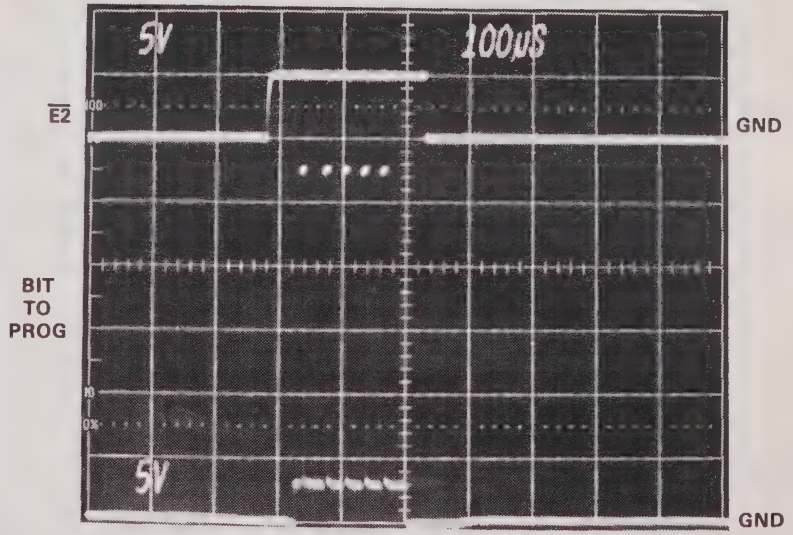
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 69, 70		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

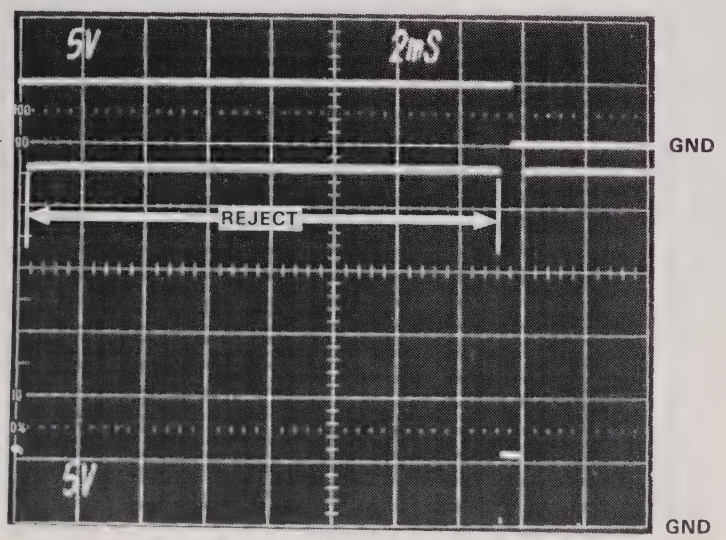
10-950-0059


5V
200µS
A0
GND
BIT
TO
PROG
5V
GND

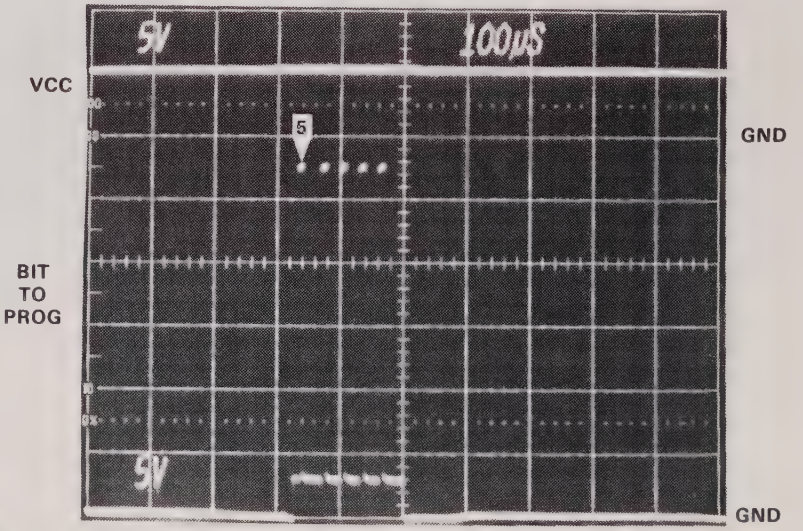
1


5V
100µS
$\overline{E2}$
GND
BIT
TO
PROG
5V
GND

2


5V
2mS
A0
GND
REJECT
BIT
TO
PROG
5V
GND

3


5V
100µS
VCC
5
GND
BIT
TO
PROG
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	µs	See Note 2
	T_R	0.28			µs	
	T_F	0.28			µs	
	Overprogram		4		Pulses	
	Reject		1000		Pulses	See Note 3
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.2	6.7	7.2	V	701-1655/TP3

NOTES

1A. Fill RAM with $FE for Family 71.
1B. Fill RAM with $01 for Family 72.
2. Measurement taken at 15V point of 01 with a 150Ω load.
3. 1,000 pulses equals 10ms as shown in photo number 3.
4. Do not use a wirewound load resistor.

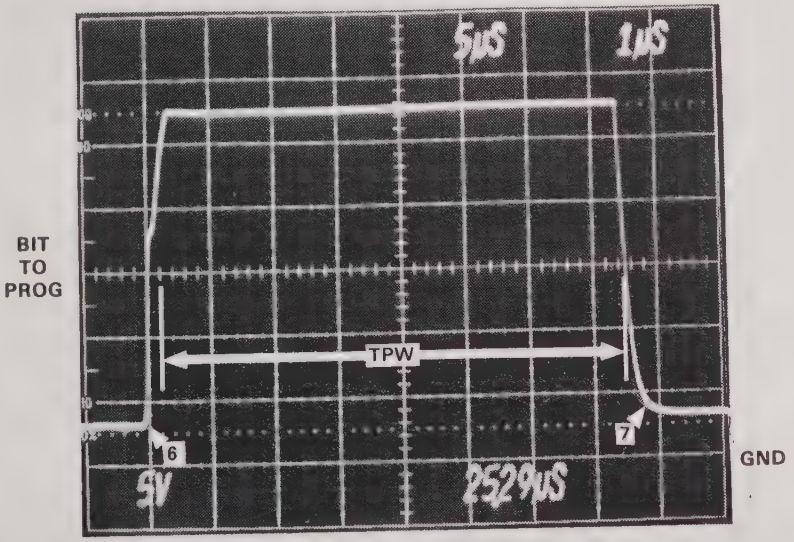
10-950-0059

REVISIONS

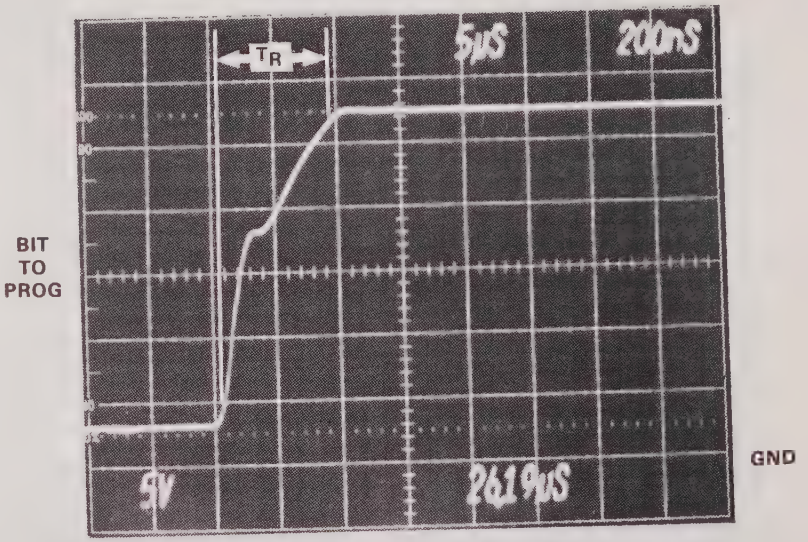
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		KH	5/6?

DATA I/O ISSAQUAH, WA

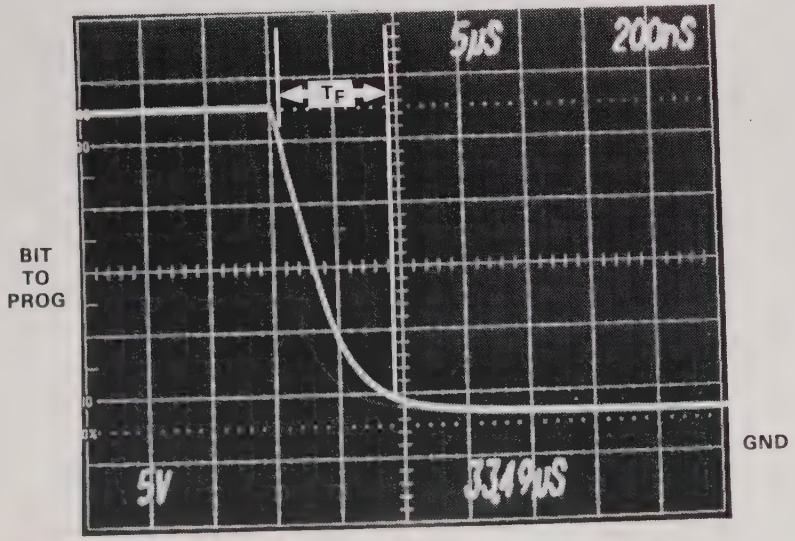
TITLE: TIMING DIAGRAM		DRAWN BY: PP
FAMILY CODES 71, 72		CHECKED BY: KH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5µS
1µS
BIT
TO
PROG
TPW
6
7
5V
2529µS
GND

5


TR
5µS
200nS
BIT
TO
PROG
5V
2619µS
GND

6


5µS
200nS
TF
BIT
TO
PROG
5V
3349µS
GND

7

GNI

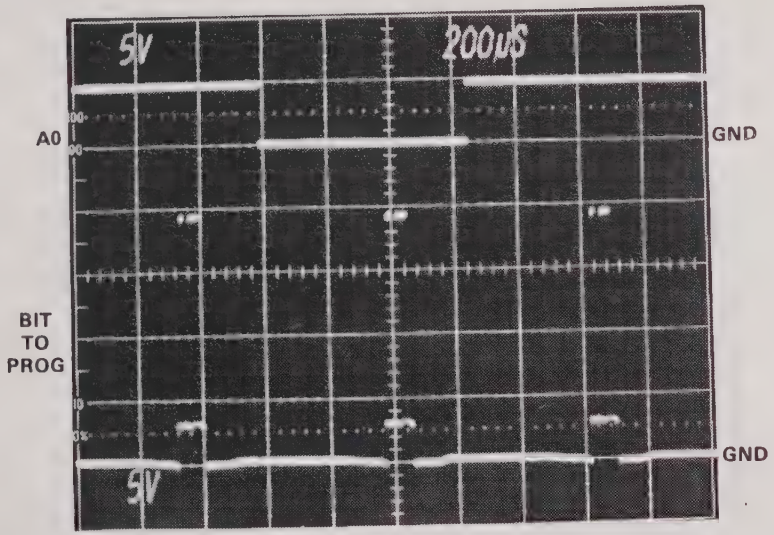
10-950-0059

REVISIONS

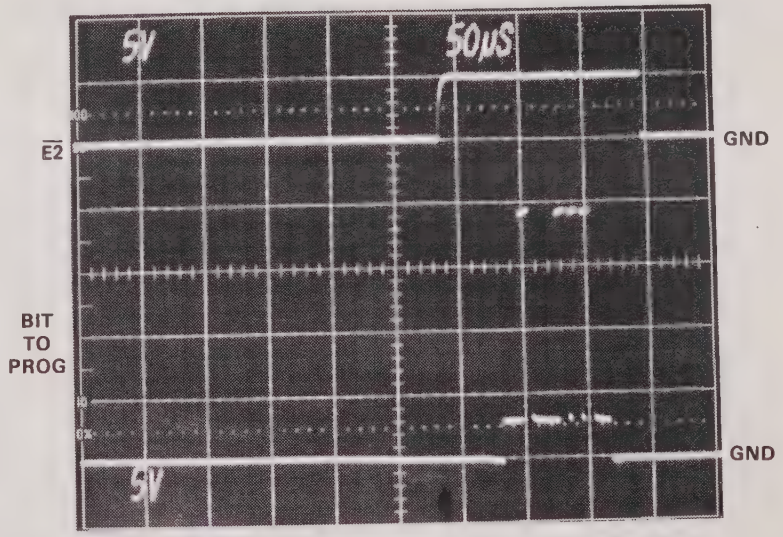
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

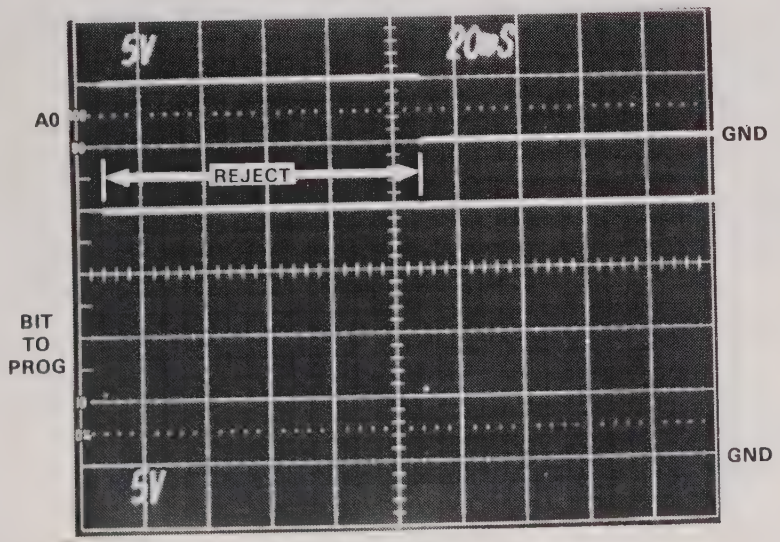
TITLE: TIMING DIAGRAM FAMILY CODES 71, 72		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

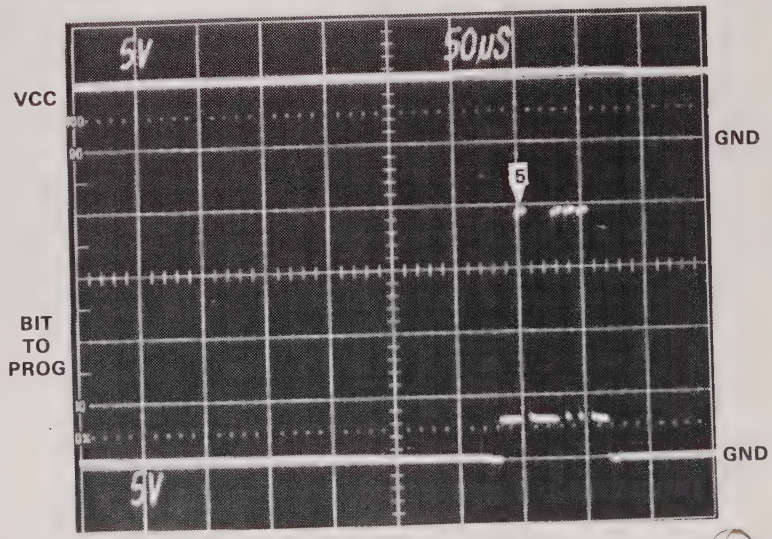
1


5V
50µS
$\overline{E2}$
GND
BIT
TO
PROG
GND
5V

2


5V
20µS
A0
GND
REJECT
BIT
TO
PROG
GND
5V

3


5V
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	
	VPP					NA
	VOP	19.6	20.0	20.0	V	
	TPW	7.1	7.5	7.9	µs	See Note 2
	TR	180			ns	
	TF	180			ns	
	Overprogram		4		Pulses	
	Reject		10000		Pulses	See Note 3
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.5	4.6	4.7	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.5	6.6	6.7	V	
	VREF	4.4	4.5	4.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.7	7.2	7.7	V	701-1655/TP3

NOTES

1A. Fill RAM with $FE for Family 73.
1B. Fill RAM with $01 for Family 74.
2. Measurement taken at 10V point of 01 with a 150Ω load.
3. 10,000 pulses equals 100ms as shown in photo number 3.
4. Do not use a wirewound load resistor.
5. For pinouts 16 and 21, E2 is seen on E1.

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 73, 74

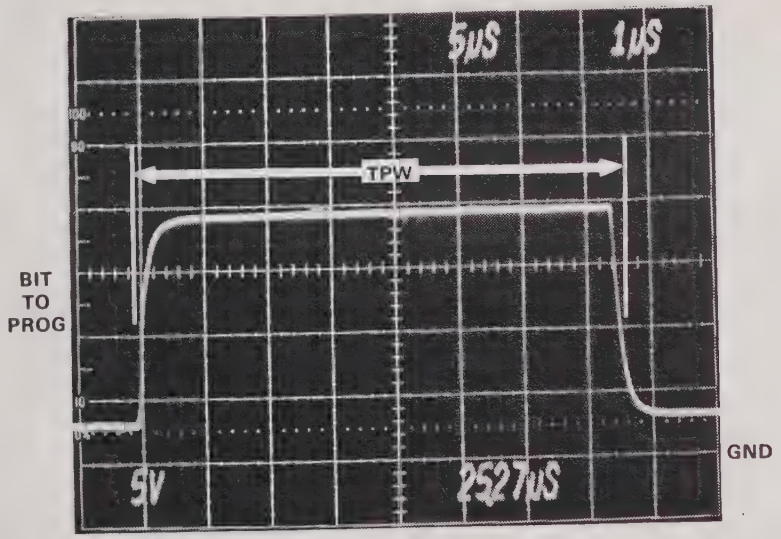
DRAWN BY: EE

CHECKED BY: XH

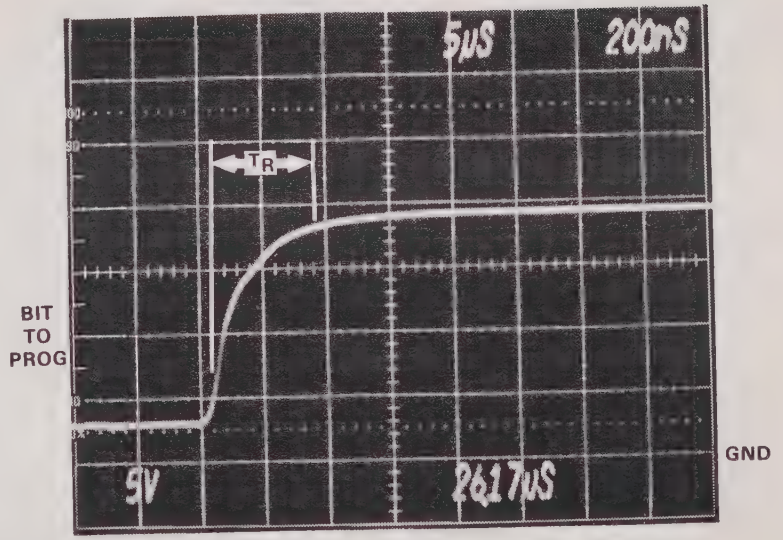
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

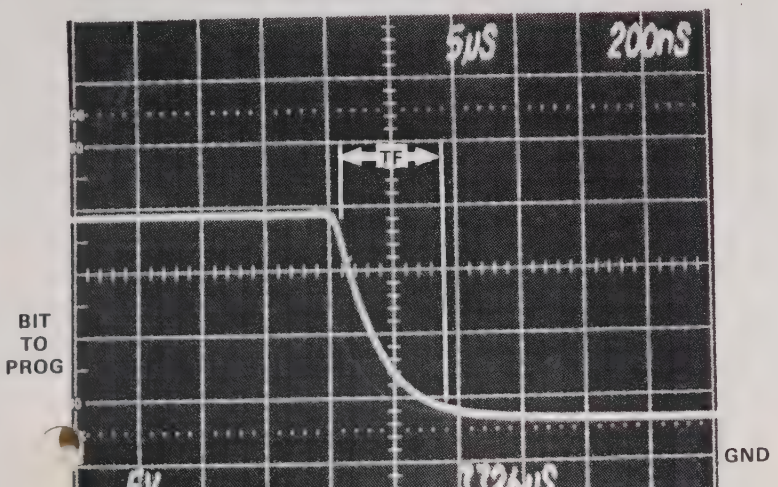
SHEET 1/2


5µS
1µS
TPW
BIT
TO
PROG
GND
9V
2527µS

5


5µS
200nS
TR
BIT
TO
PROG
GND
9V
2617µS

6


5µS
200nS
TF
BIT
TO
PROG
GND

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE: **TIMING DIAGRAM**

FAMILY CODES 73, 74

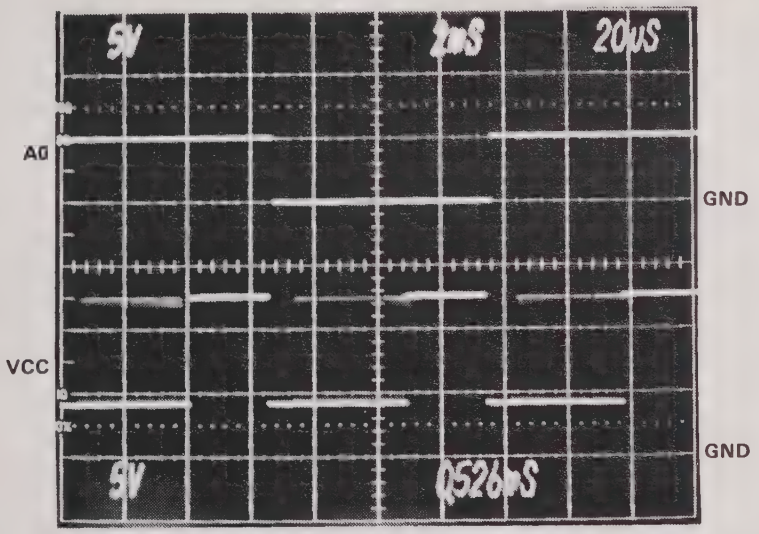
DRAWN BY: EE

CHECKED BY: XH

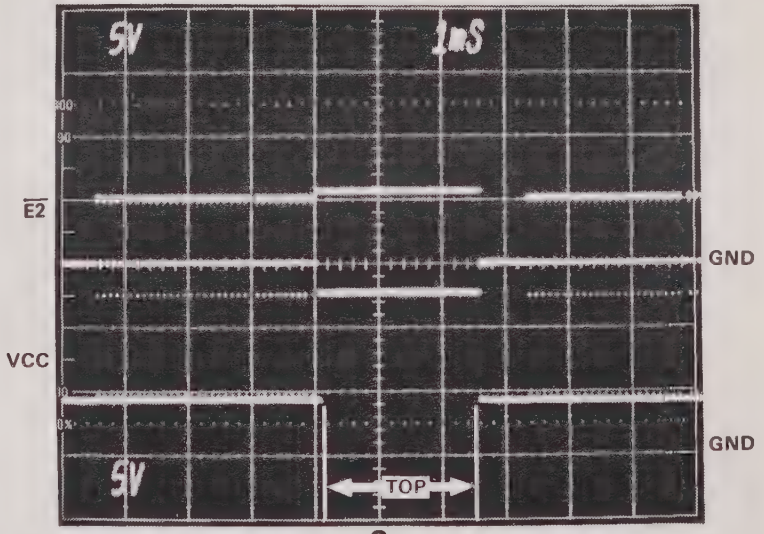
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

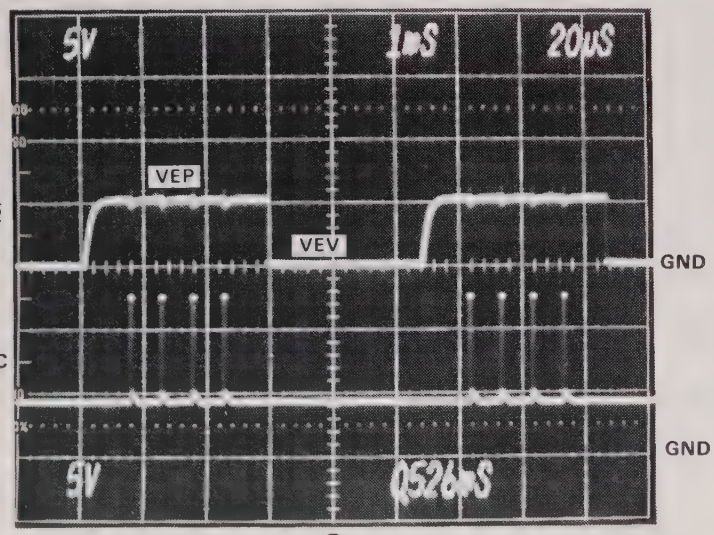
SHEET 2/2


5V
1mS
20μS
A0
GND
VCC
GND
5V
0526mS

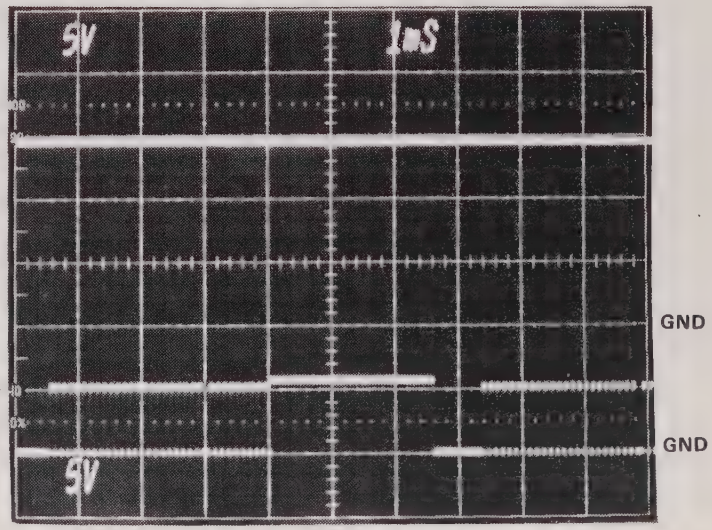
1


5V
1mS
E2
GND
VCC
GND
5V
TOP

2


5V
1mS
20μS
VEP
E2
VEV
GND
VCC
GND
5V
0526mS

3


5V
1mS
E3
GND
E2
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12.0	12.5	13.0	V	See Note 6
	VCCV	4.25	4.5	4.75	V	
	VEP	3.0	5.0	5.5	V	
	VEV	0.0	0.2	0.4	V	
	TPWB	140	200	260	ns	See Note 4
	TPWE	7.2	8.0	8.8	µs	See Note 4
	TR	320	400	480	ns	See Note 5
	TF	50	100	200	ns	See Note 5
	Reject	780	800	820	ms	
	TOP	2.2	2.5	2.8	ms	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.4	0.5	0.6	V	701-1655/TP2
	High Load	17.8	18.8	19.8	V	701-1655/TP4
	Low Load	17.8	18.8	19.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.2	2.3	2.4	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.9	7.9	8.9	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for family 75.*
2. *Load RAM with $01 for family 76.*
3. *To observe waveforms, load 01 with a 100Ω , 2 watt resistor. Do not use a wirewound resistor.*
4. *VCC pulse width ramps linearily from TPWB to TPWE. This is visible only with no load on 01. TPW is measured at 12V.*
5. *TR and TF are measured from 5V to 12V.*
6. *Photos 5 and 6 were taken with VCC loaded with a 50Ω , 5 watt resistor. Do not use a wirewound resistor.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	B	ECN #4772		XH	1/83
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 75, 76

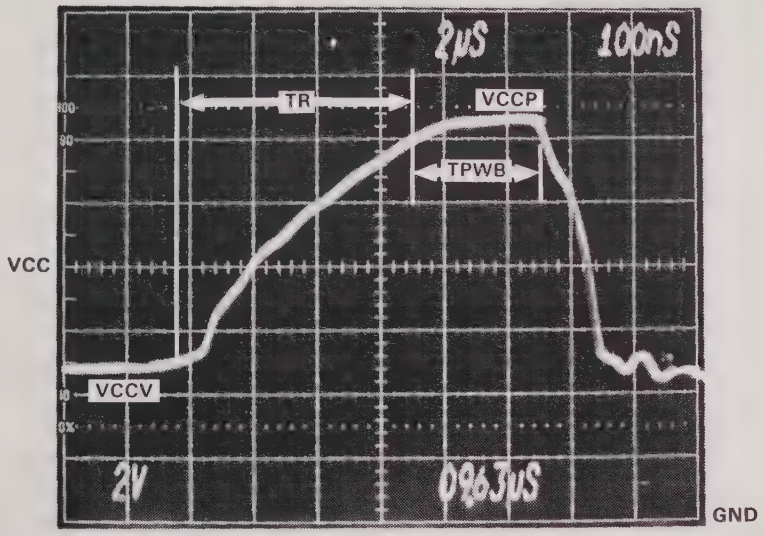
DRAWN BY: BG

CHECKED BY:

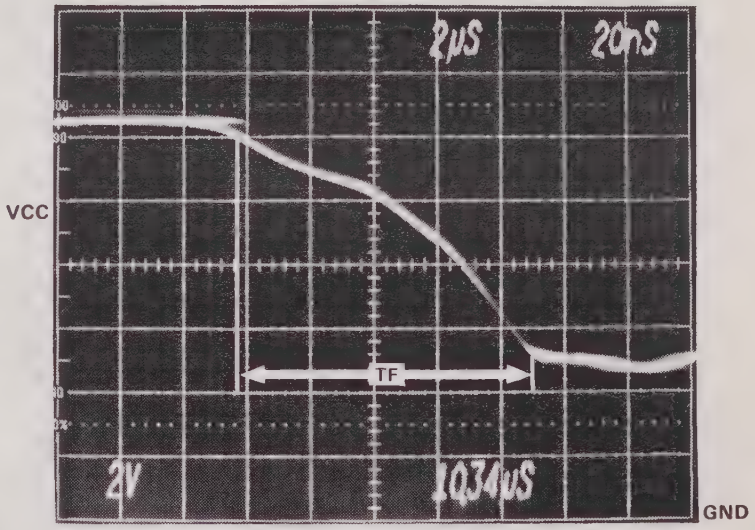
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


2µS
100nS
TR
VCCP
TPWB
VCC
VCCV
2V
0963µS
GND

5


2µS
20nS
VCC
TF
2V
1034µS
GND

6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJJ	11/82
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 75, 76

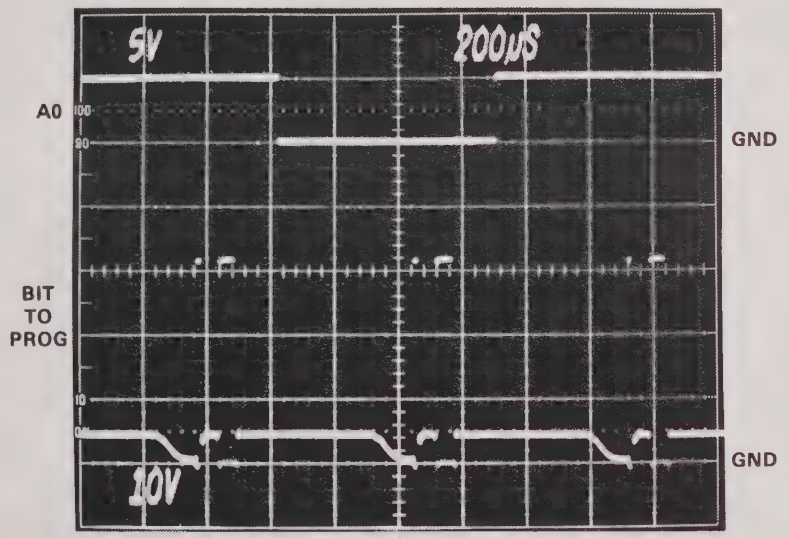
DRAWN BY: BCJ KH

CHECKED BY:

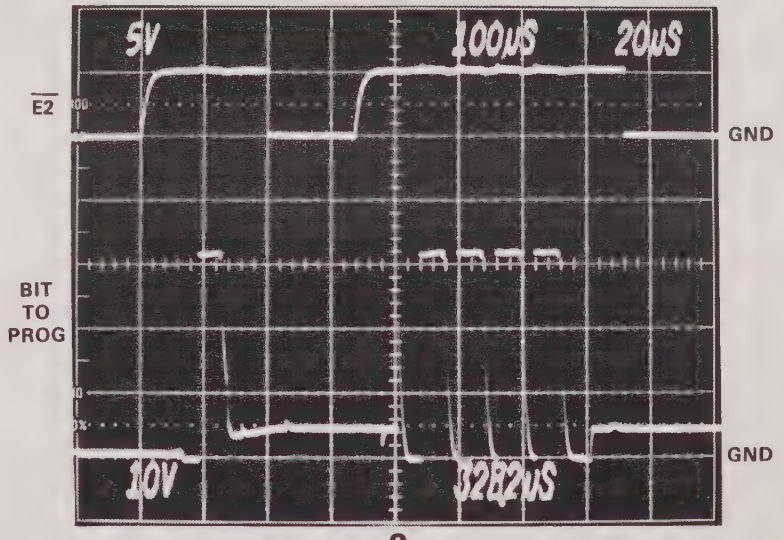
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

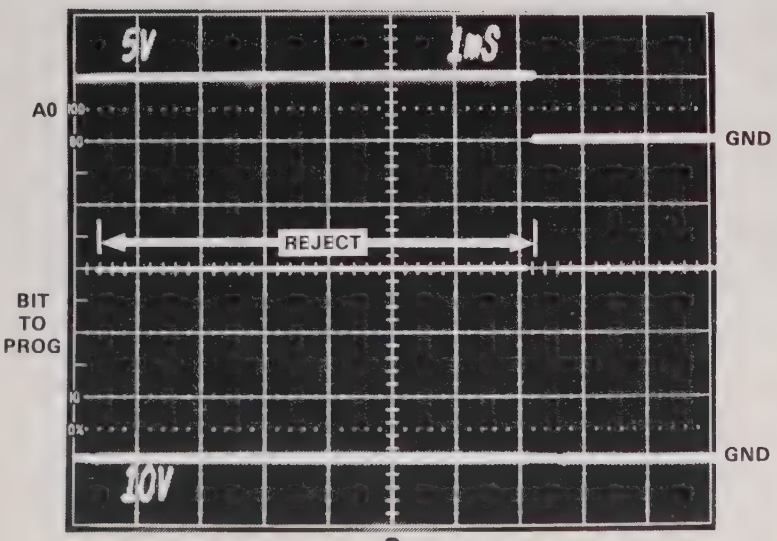
SHEET 2/2


5V
200µS
A0
GND
BIT
TO
PROG
GND
10V

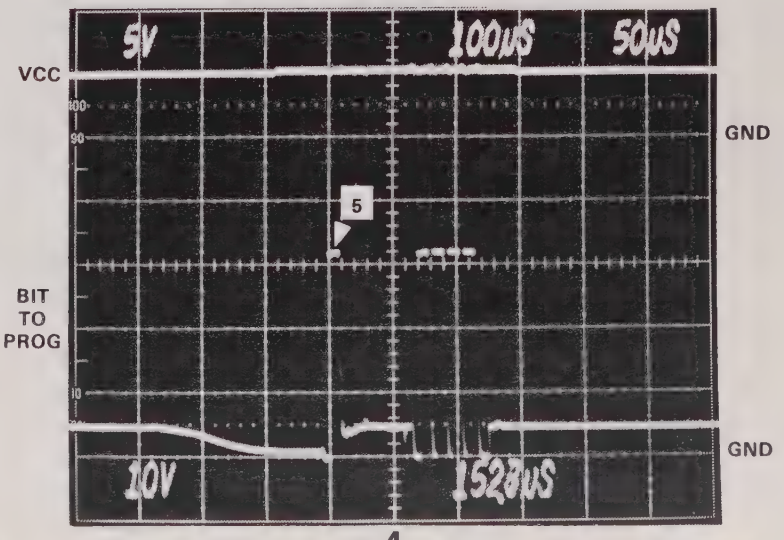
1


5V
100µS
20µS
E2
GND
BIT
TO
PROG
GND
10V
3282µS

2


5V
1mS
A0
GND
REJECT
BIT
TO
PROG
GND
10V

3


5V
100µS
50µS
VCC
GND
5
BIT
TO
PROG
GND
10V
1528µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	
	VPP					NA
	VOP	31.5	31.7	32.0	V	
	TPN	7.2	7.5	7.8	µs	See Note 2
	TR	0.34		0.68	µs	
	TF	0.34		0.48	µs	
	Overprogram		4		Pulses	
	Reject		100		Pulses	See Note 3
	Duty Cycle	11			%	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	7.8	8.8	9.8	V	701-1655/TP4
	Low Load	7.8	8.8	9.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	5.6	6.6	7.6	V	701-1655/TP3

NOTES

1A. Fill RAM with $FE for Family 77.
1B. Fill RAM with $01 for Family 78.
2. Measurement taken at 15v point of 01 with 150Ω load.
3. 100 pulses equals 6.8ms as shown in photo number 3 with 150Ω load.
4. Do not use a wirewound load resistor.
5. Photos 1, 2, and 4 have 01 loaded with 3.3kΩ.

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJZ	11/82
	B	ECN #4772		XX	1/83
	C	ECN #4831		ZH	5/83

DATA I/O ISSAQUAH, WA

TITLE: **TIMING DIAGRAM**

FAMILY CODES 77, 78

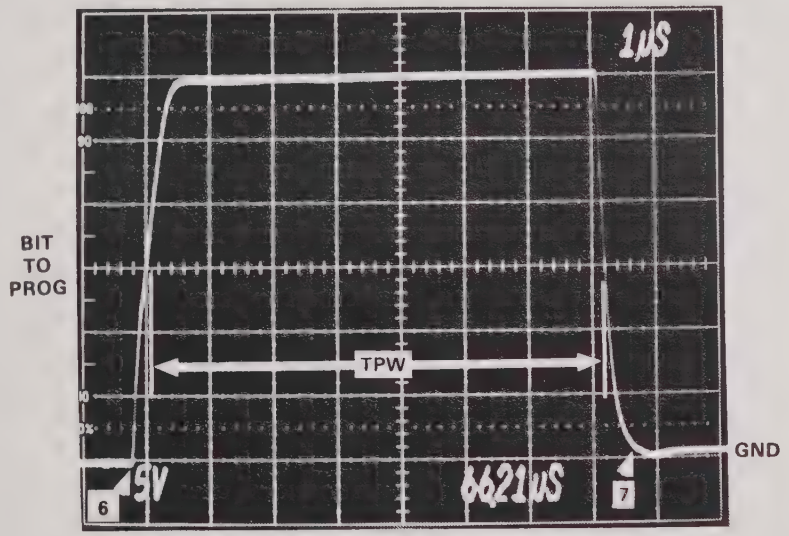
DRAWN BY: EE

CHECKED BY:

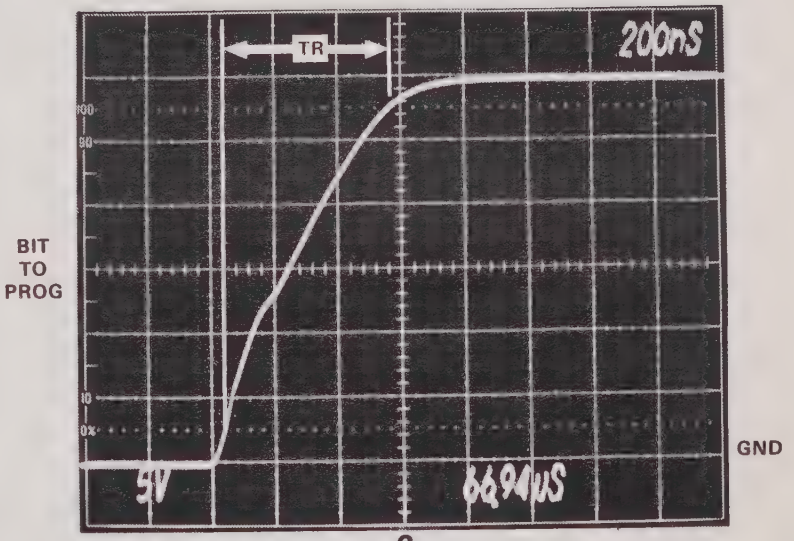
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

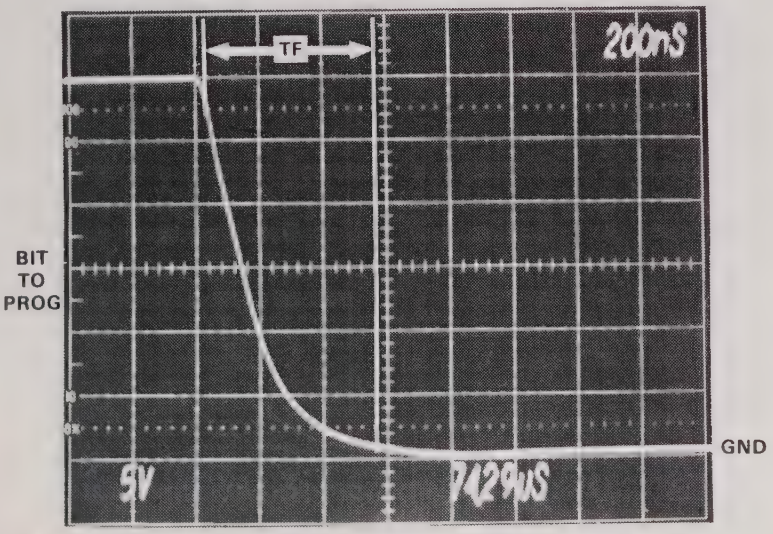
SHEET 1/2


1µS
BIT
TO
PROG
TPW
GND
5V
6621µS
6
7

5


TR
200nS
BIT
TO
PROG
GND
5V
6694µS

6


TF
200nS
BIT
TO
PROG
GND
5V

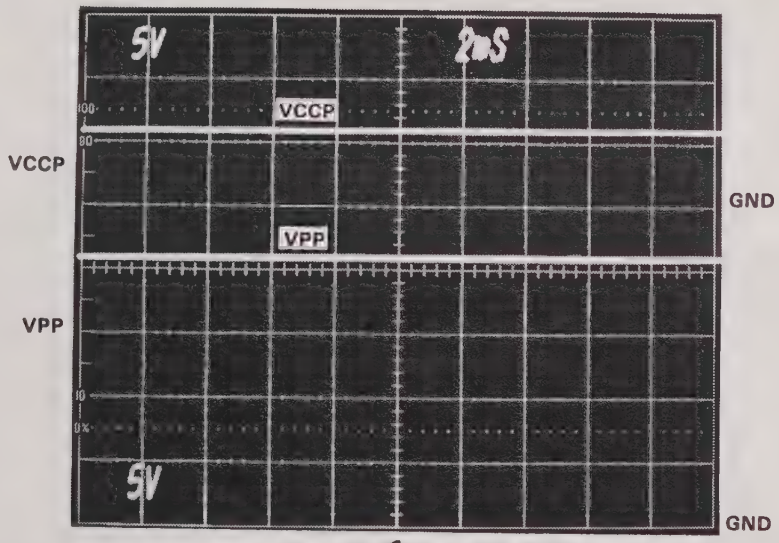
7

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		ZH	5/83

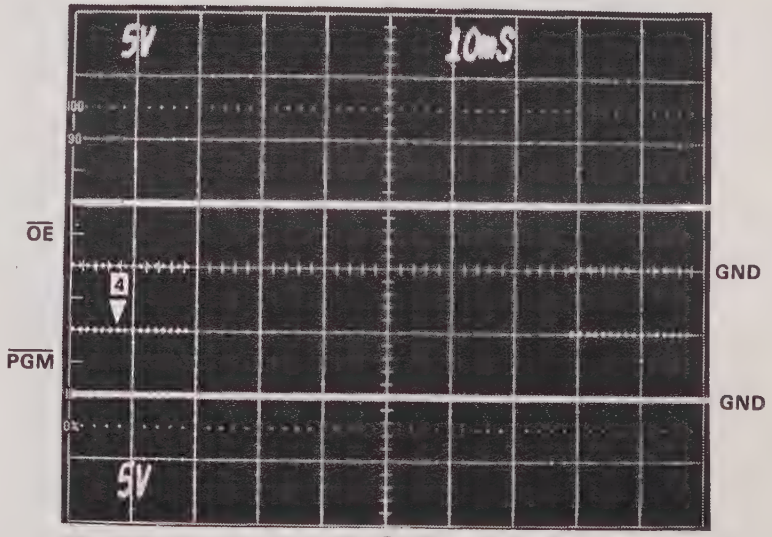
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 77, 78		DRAWN BY: EE CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

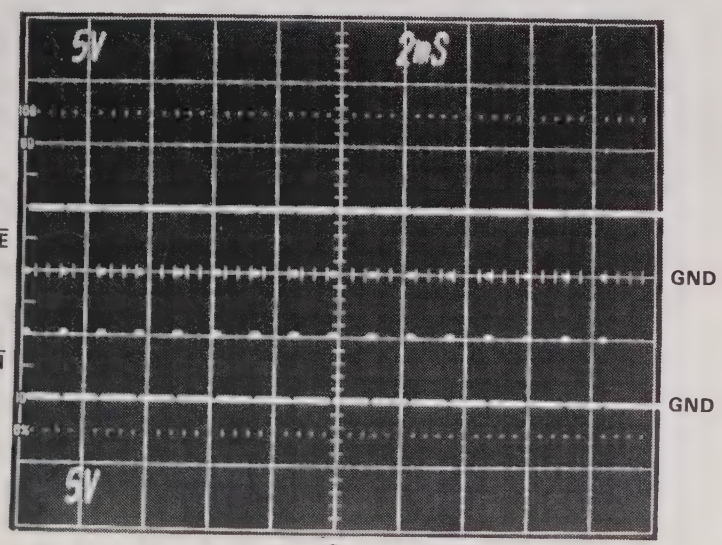
10-950-0059



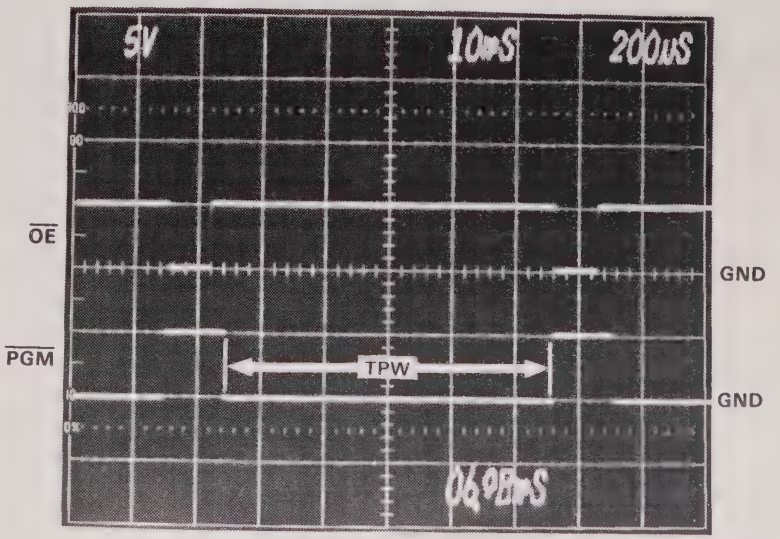
1



2



3



4

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		15		Pulses	
	Overprogram		1		Pulses	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

1. *Load RAM with $FE for Family 79.*
2. *Load RAM with $01 for Family 80, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *The overprogram pulse follows the reject pulses and its length is the number of reject pulses multiplied by 4 ms.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		KH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 79, 80

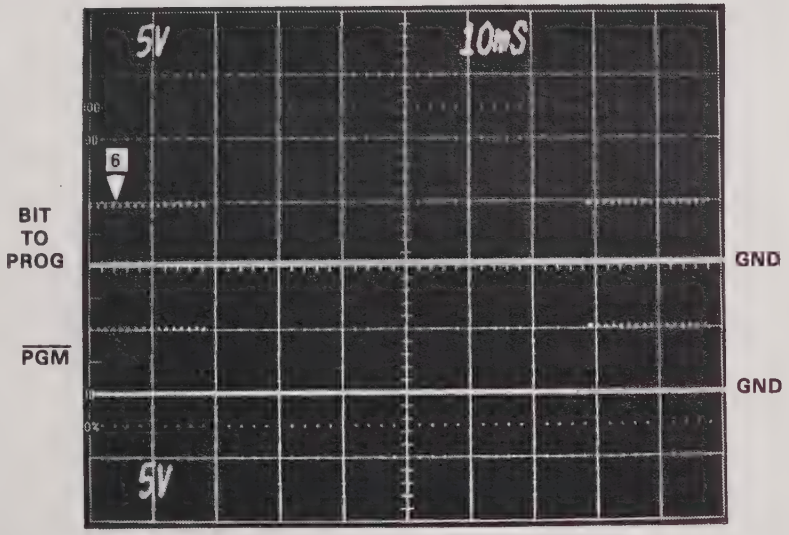
DRAWN BY: BG KH

CHECKED BY:

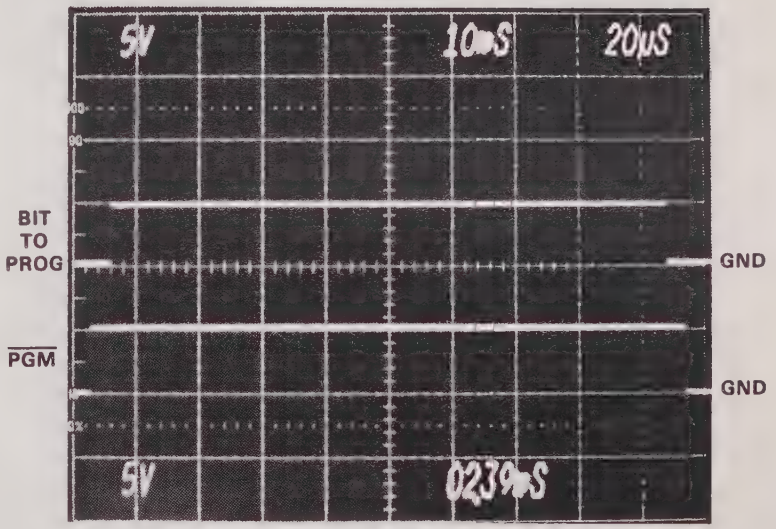
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

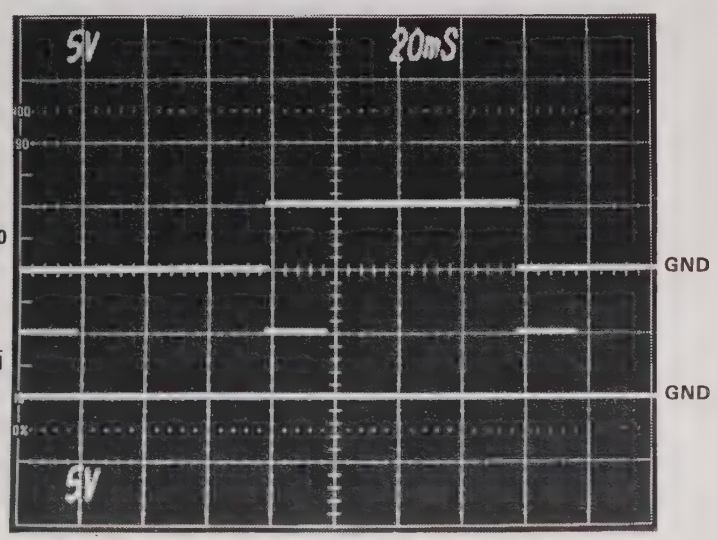
SHEET 1/2


5V
10mS
6
BIT
TO
PROG
GND
PGM
GND
5V

5


5V
10mS
20µS
BIT
TO
PROG
GND
PGM
GND
5V

6


5V
20mS
A0
GND
PGM
GND
5V

7

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		KH	5/83

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 79, 80

DRAWN BY: [signature]

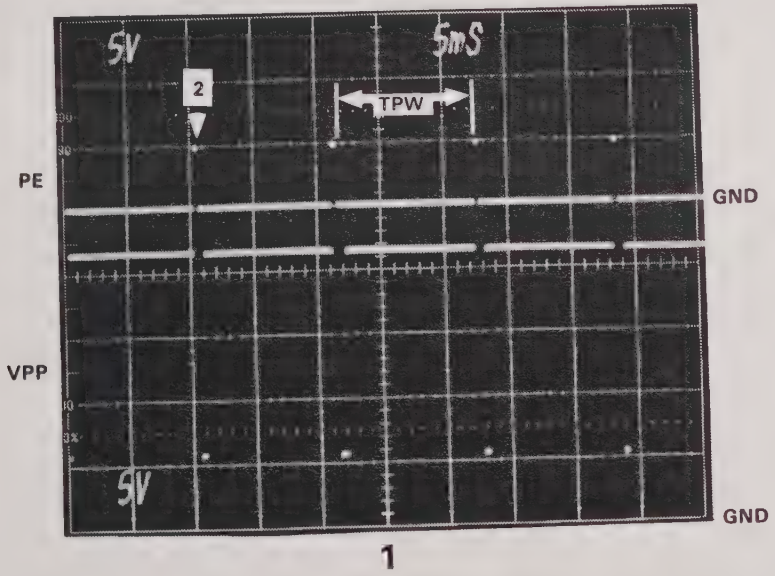
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

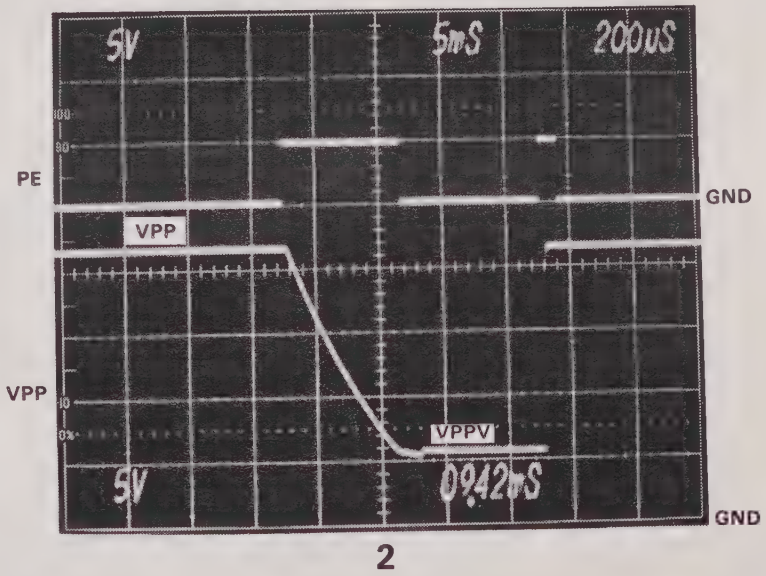
SCALE

SHEET 2/2

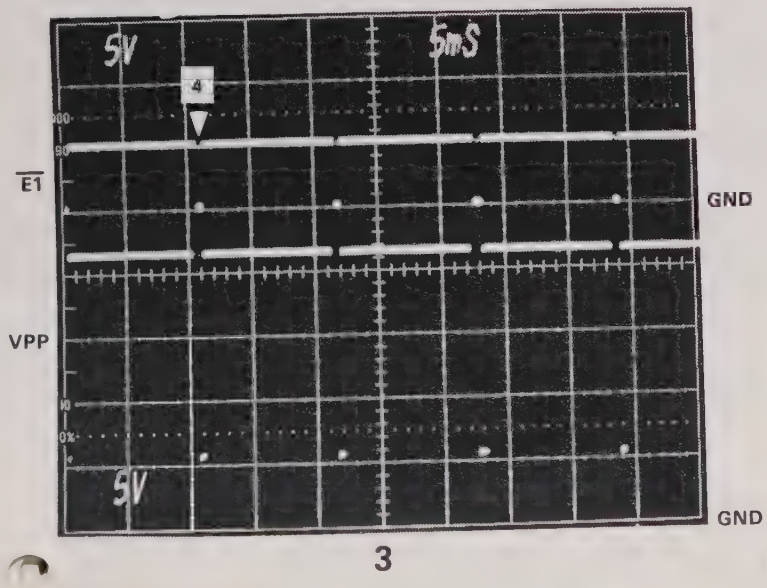
10-950-0059


5V
5mS
2
TPW
PE
GND
VPP
5V
GND

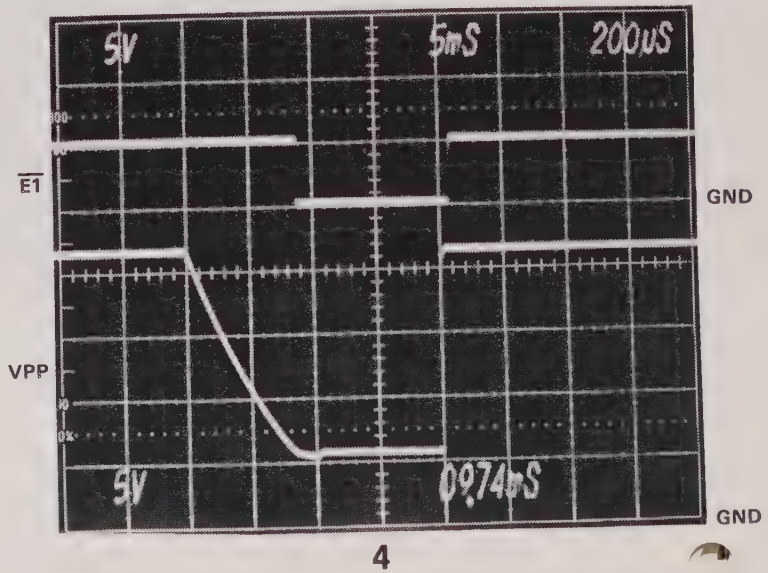
1


5V
5mS
200uS
PE
GND
VPP
VPP
VPPV
5V
09.42mS
GND

2


5V
5mS
4
E1
GND
VPP
5V
GND

3


5V
5mS
200uS
E1
GND
VPP
5V
09.74mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	1			µs	
	TF	1			µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 81.*
2. *Load RAM with $01 for Family 82, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *Photos 13 thru 18 are erase waveforms.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		XP	5/83

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES 81, 82

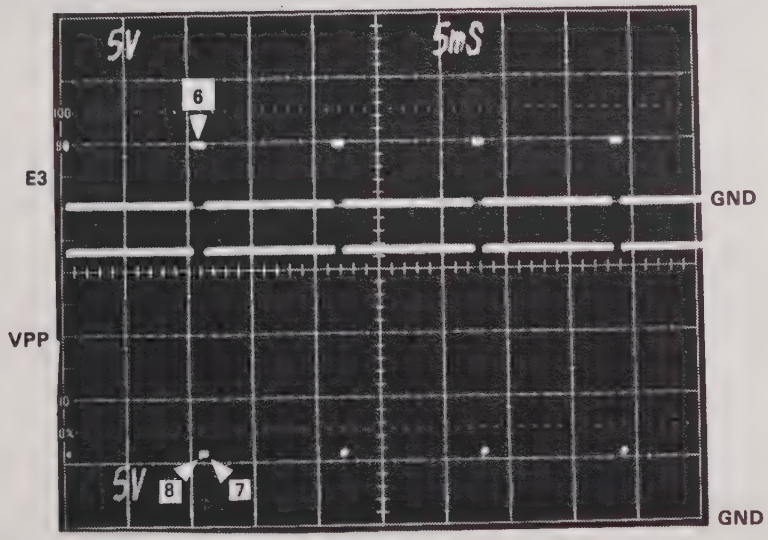
DRAWN BY:

CHECKED BY:

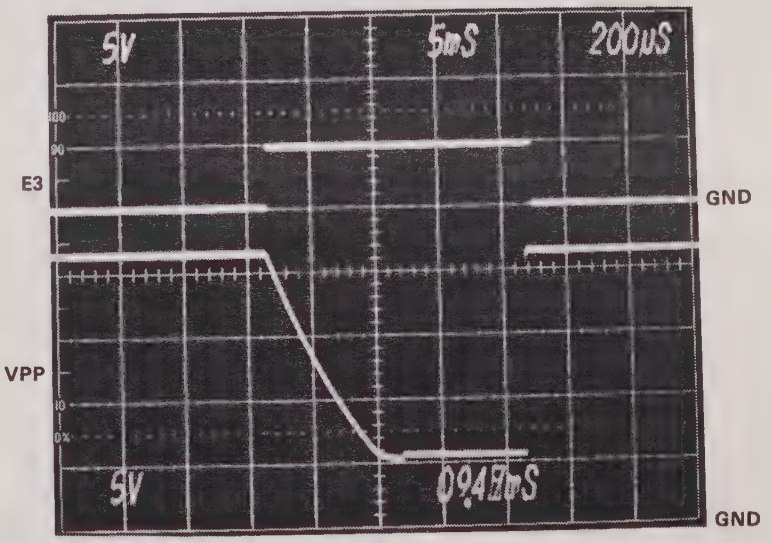
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

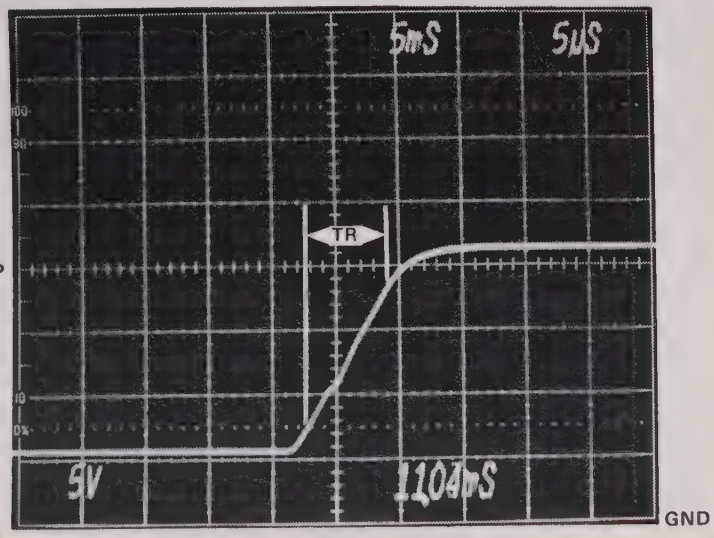
SHEET 1/4


5V
5mS
6
E3
GND
VPP
5V
8
7
GND

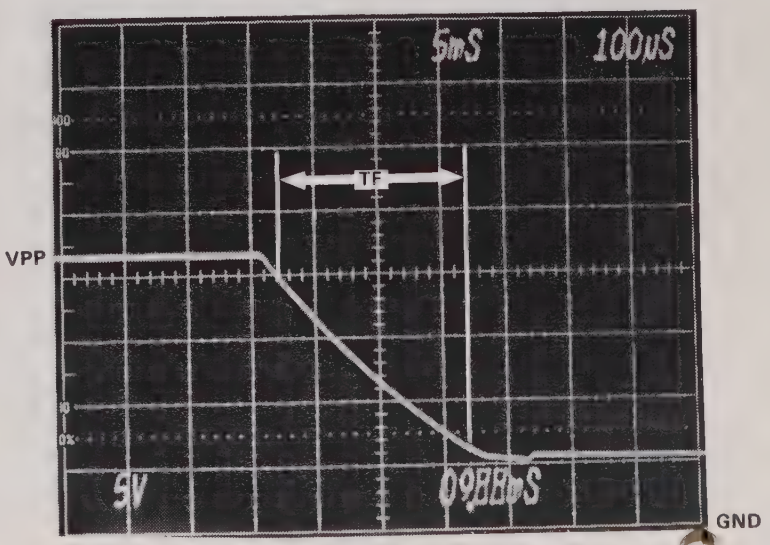
5


5V
5mS
200uS
E3
GND
VPP
5V
GND

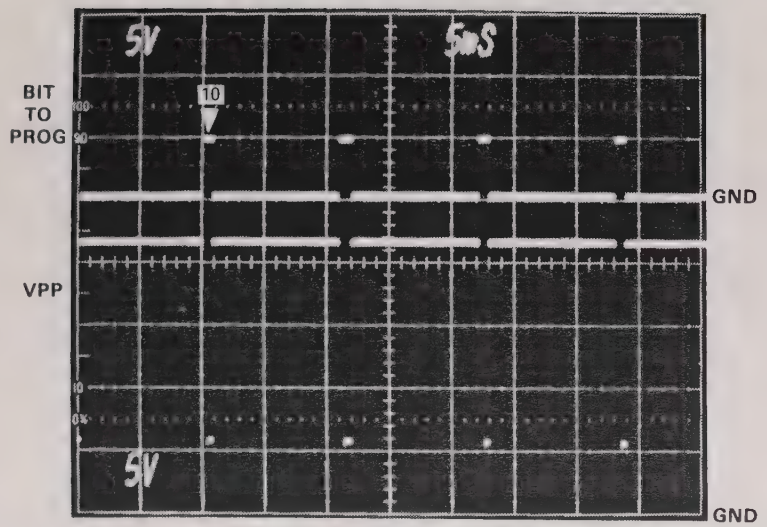
6


5mS
5uS
TR
VPP
5V
GND

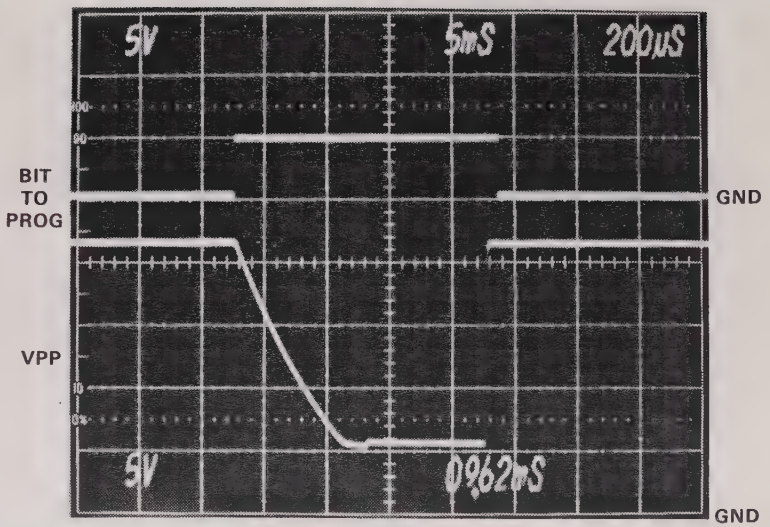
7


5mS
100uS
TF
VPP
5V
GND

8



9



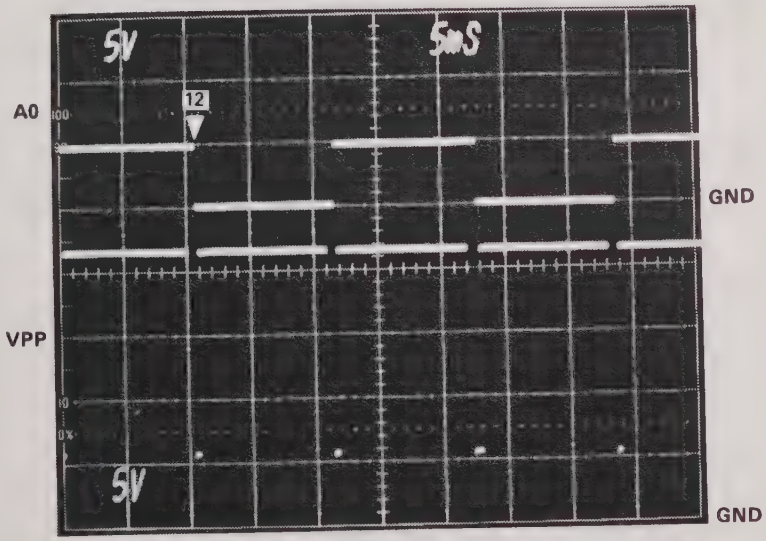
10

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.J.	11/82
	C	ECN #4831		[illegible]	[illegible]

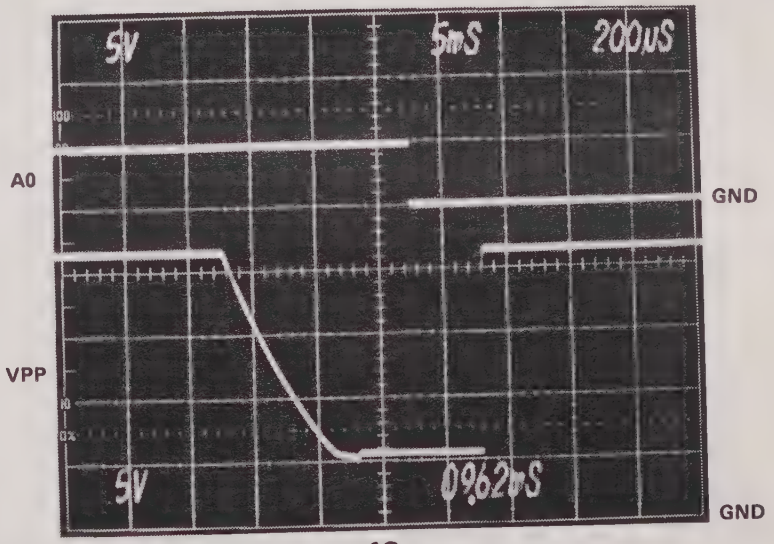
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM			DRAWN BY:
FAMILY CODES 81, 82			CHECKED BY:
SIZE	CODE IDENT. NO.	DRAWING NO.	
B	54193	33-950-0059	
SCALE			SHEET 2/4

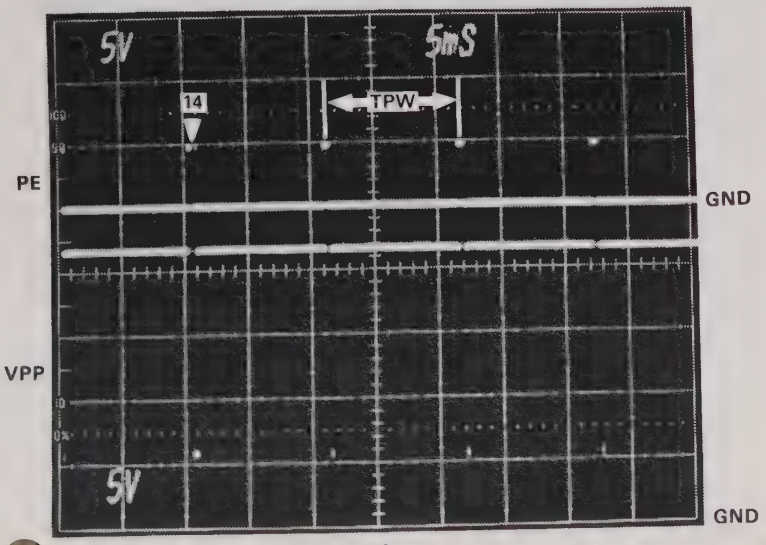
10-950-0059


5V
5mS
A0
12
GND
VPP
5V
GND

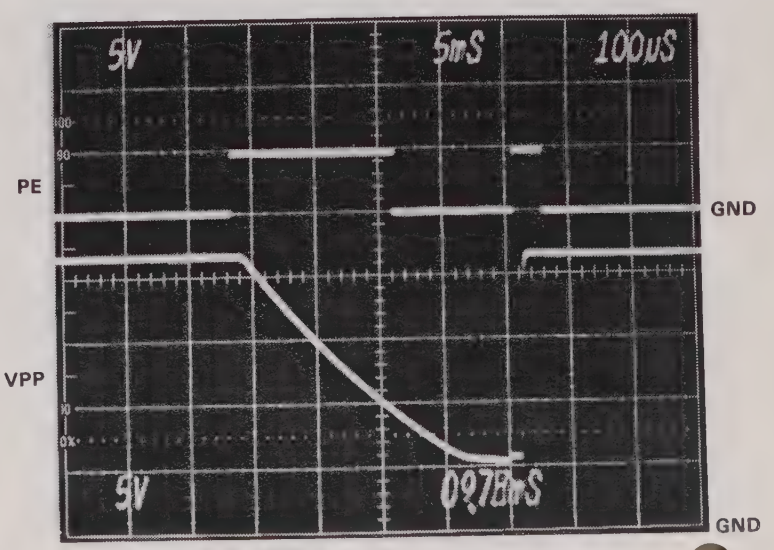
11


5V
5mS
200uS
A0
GND
VPP
5V
0.962mS
GND

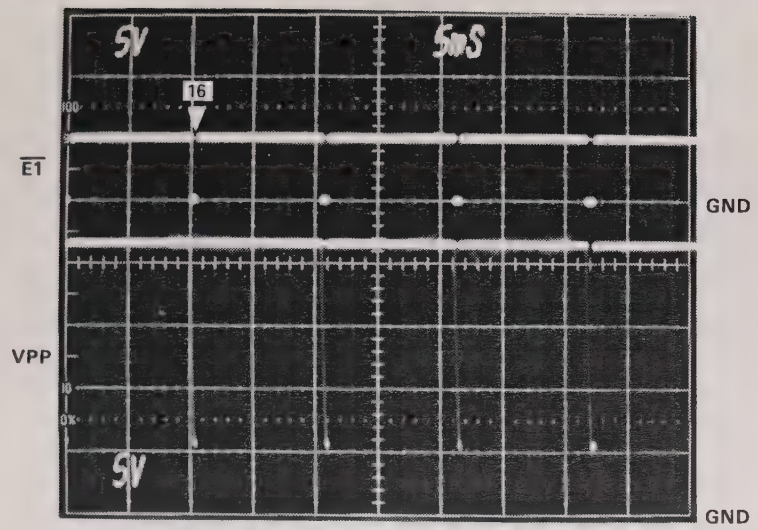
12


5V
5mS
14
TPW
PE
GND
VPP
5V
GND

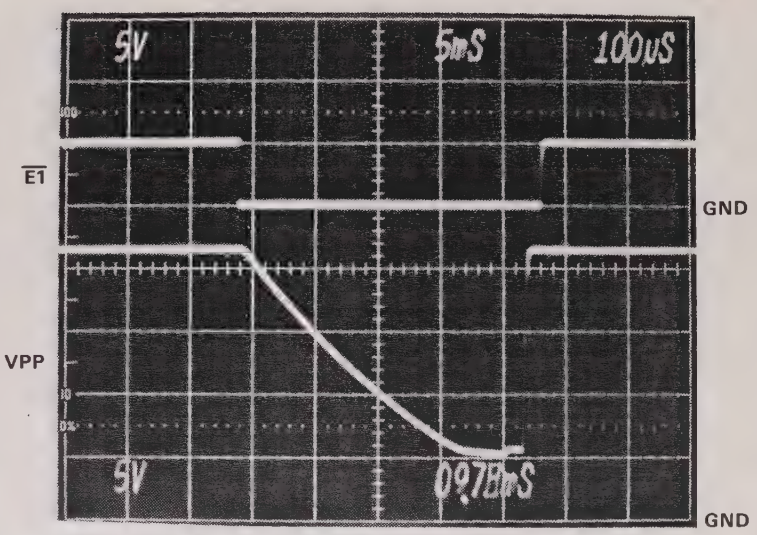
13


5V
5mS
100uS
PE
GND
VPP
5V
0.978mS
GND

14



15



16

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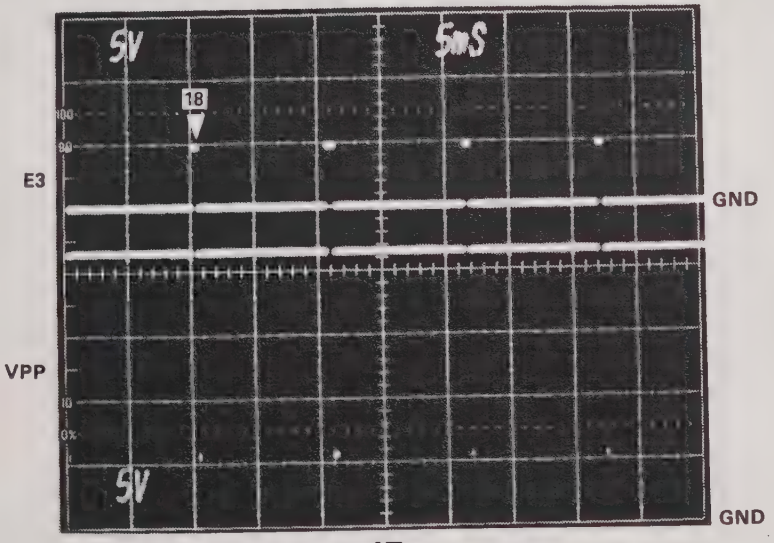
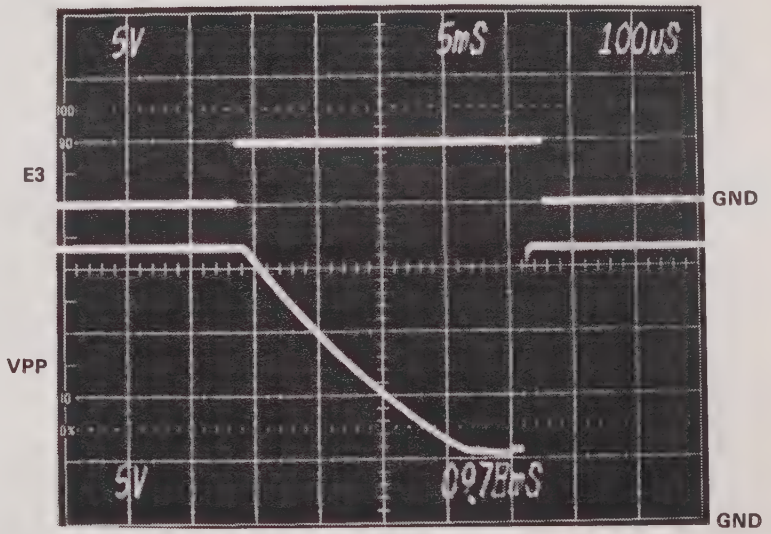
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJZ.	11/82
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 81, 82		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3/4



17



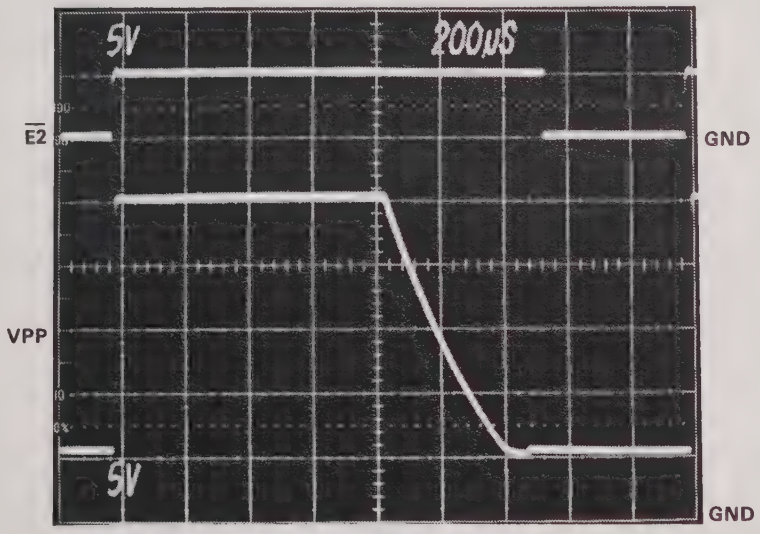
18

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJZ	11/82
	C	ECN #4831		XX	5/83

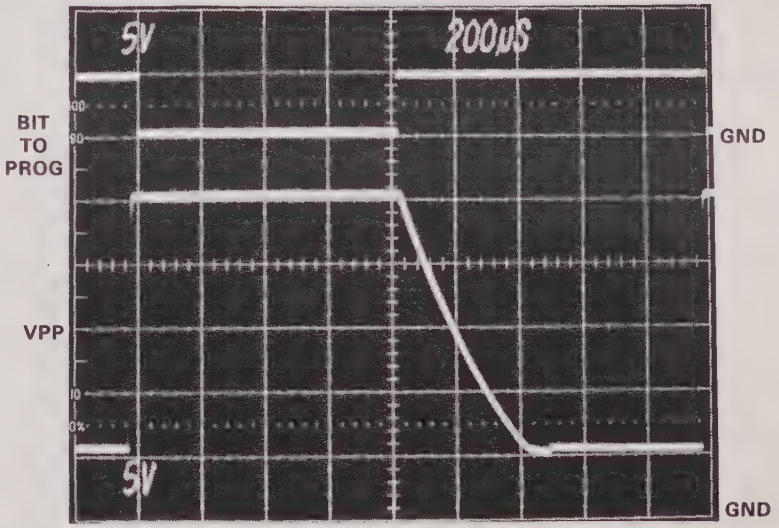
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 81, 82		DRAWN BY: KC CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 4/4

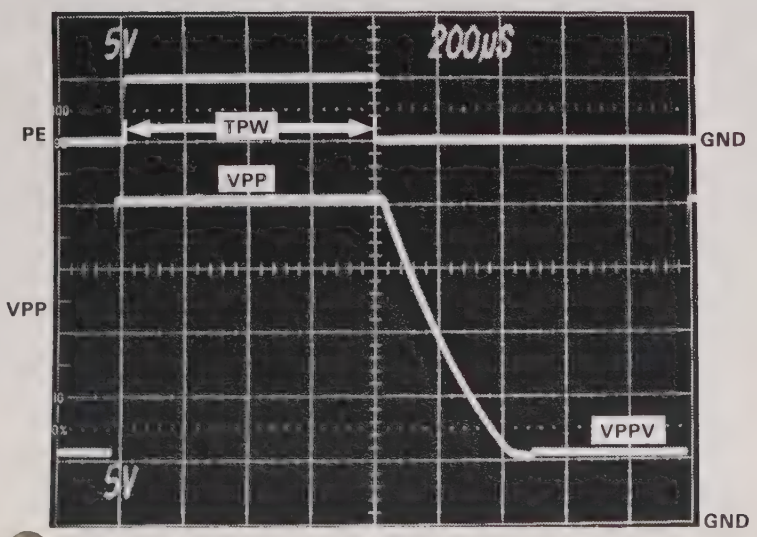
10-950-0059


5V
200µS
$\overline{E2}$
GND
VPP
5V
GND

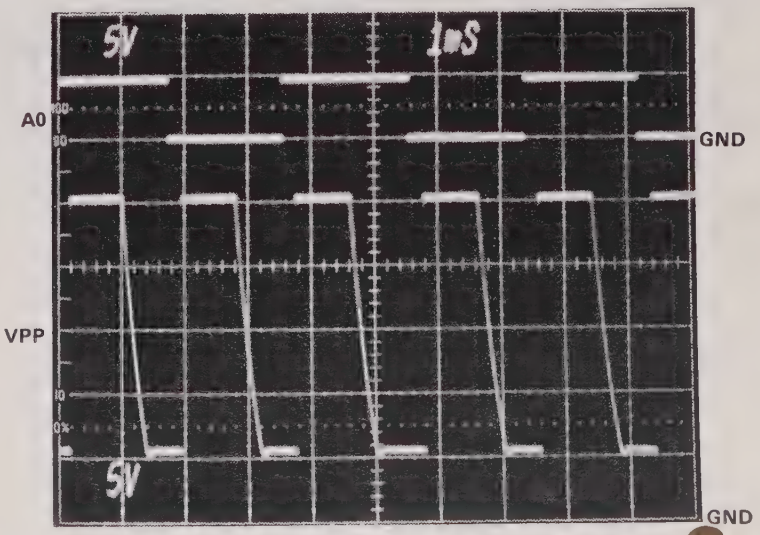
1


5V
200µS
BIT
TO
PROG
GND
VPP
5V
GND

2


5V
200µS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

3


5V
1µS
A0
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	800			µs	
	TR	5			ns	
	TEP	1			sec	
	TF	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 83.*
2. *Load RAM with $01 for Family 84, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *Photo 7 is the erase waveform.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 83, 84

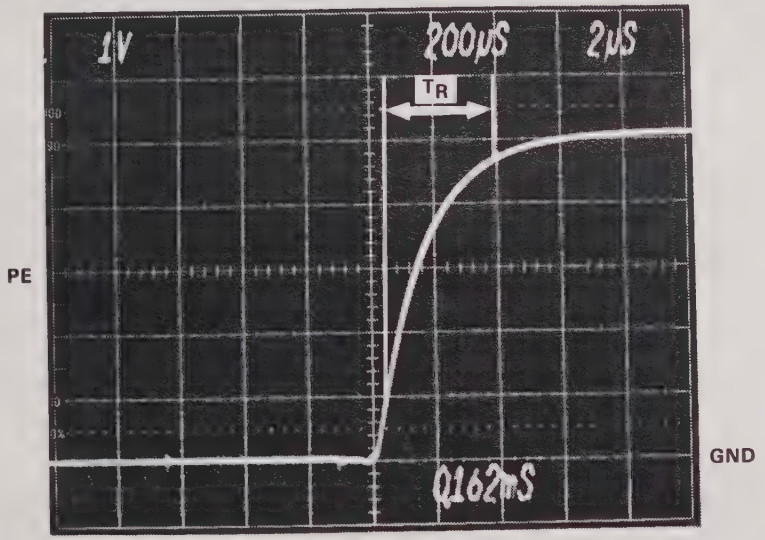
DRAWN BY:

CHECKED BY:

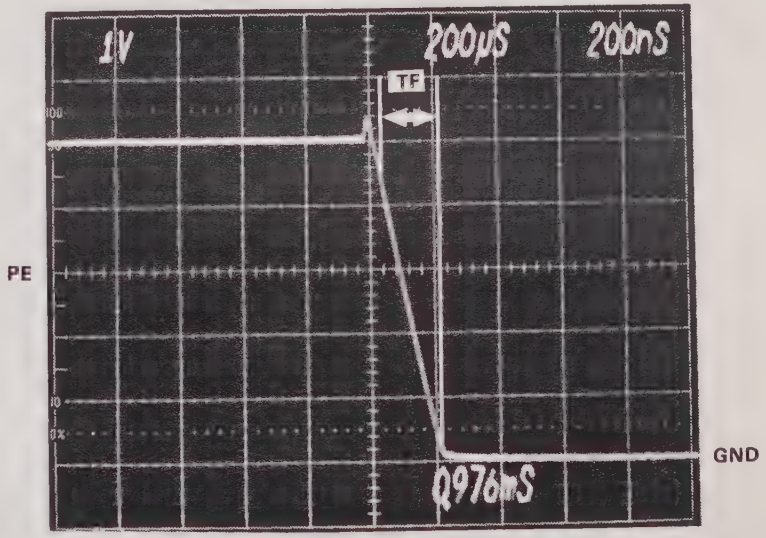
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

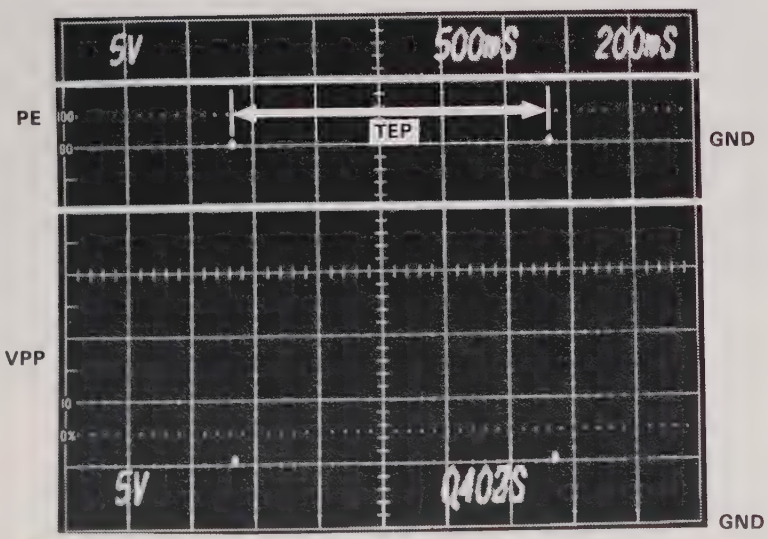
SHEET 1/2



5



6



7

10-950-0059

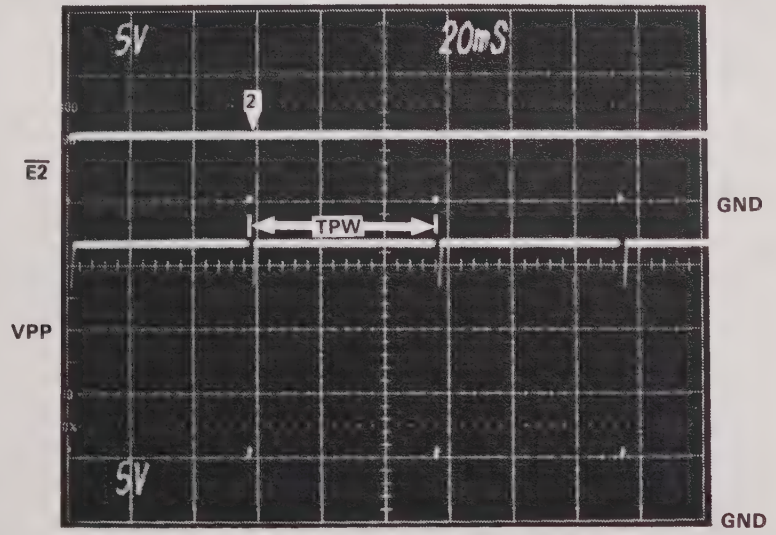
10-950-0059

REVISIONS

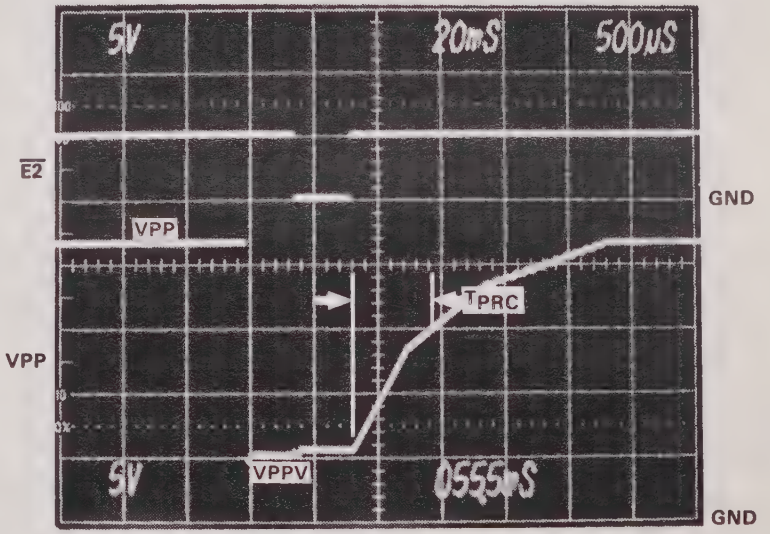
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		E.T.J.	11/82
	C	ECN #4831		XA	5/83

DATA I/O ISSAQUAH, WA

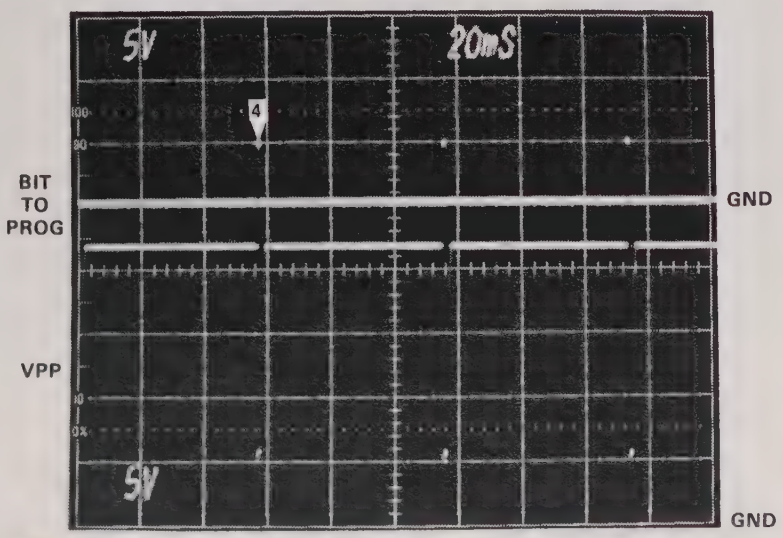
TITLE: TIMING DIAGRAM FAMILY CODES 83, 84		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
20mS
2
$\overline{E2}$
TPW
GND
VPP
5V
GND

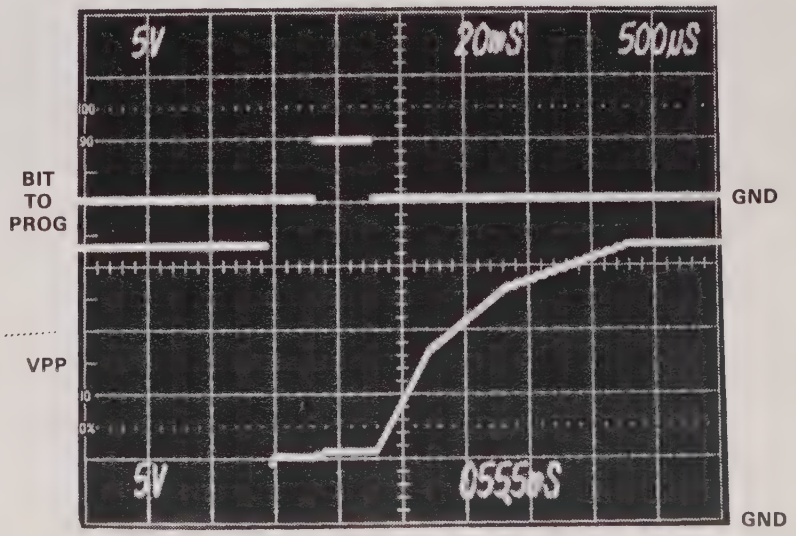
1


5V
20mS
500µS
$\overline{E2}$
GND
VPP
TPRC
VPP
VPPV
5V
0555mS
GND

2


5V
20mS
4
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
20mS
500µS
BIT
TO
PROG
GND
VPP
5V
0555mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VEE	9.0		15.0	V	
	TPW	50		70	ms	
	T_{PRC}	450	600	750	µs	See note 3
	T_F			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 85.*
2. *Load RAM with $01 for Family 86, and Bit-to-Prog waveform becomes Bit-no-Prog.*
3. *TPRC is measured from 6V to 15.5V.*
4. *Photos 8 and 9 are erase waveforms.*

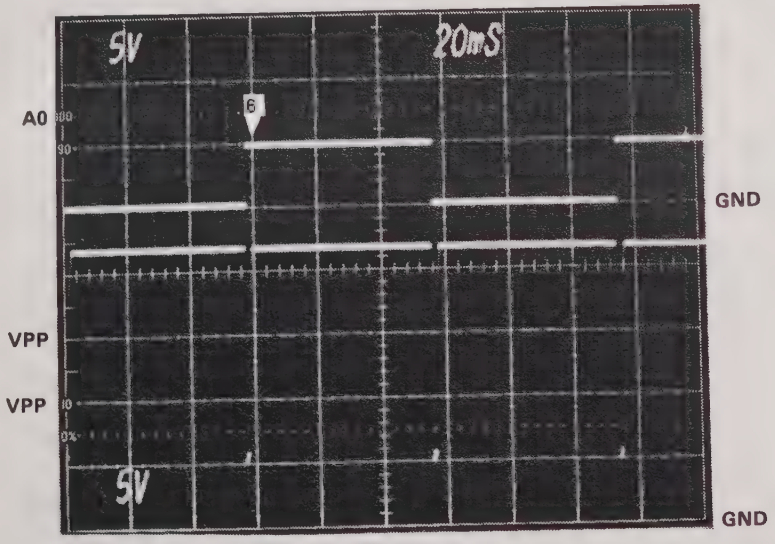
10-950-0059

REVISIONS

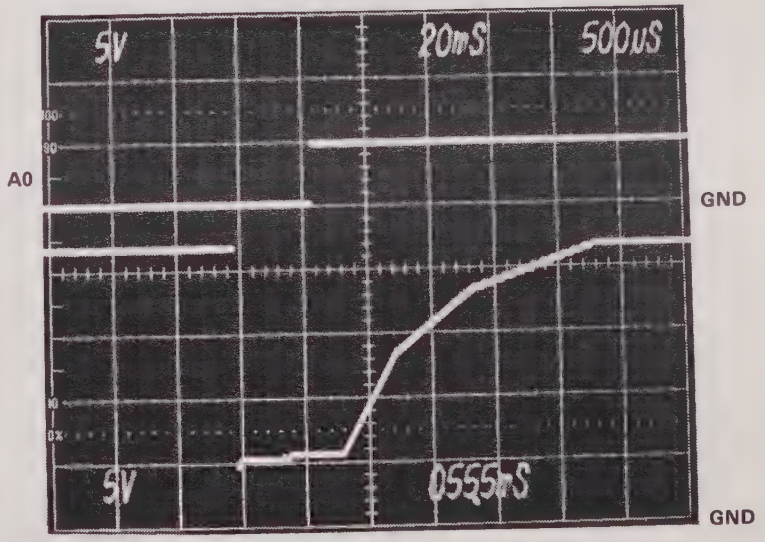
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		CJZ	11/82
	C	ECN #4831		KH	5/83

DATA I/O ISSAQUAH, WA

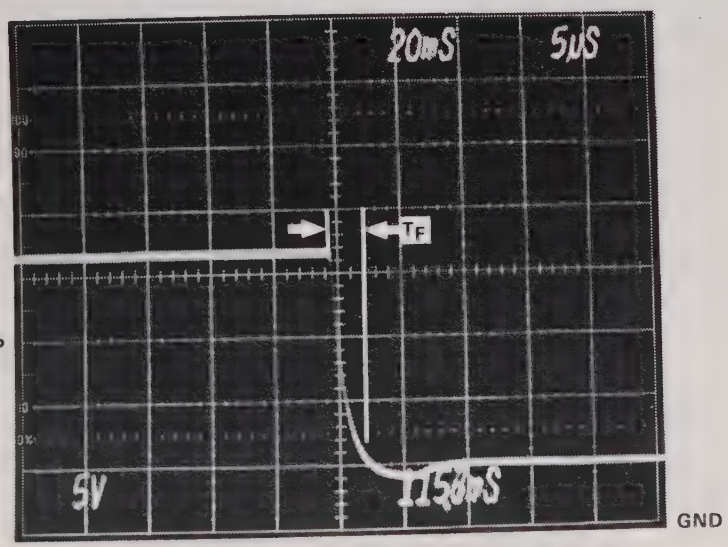
TITLE: TIMING DIAGRAM		DRAWN BY: KH
FAMILY CODES 85, 86		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5V
20mS
A0
6
GND
VPP
VPP
5V
GND

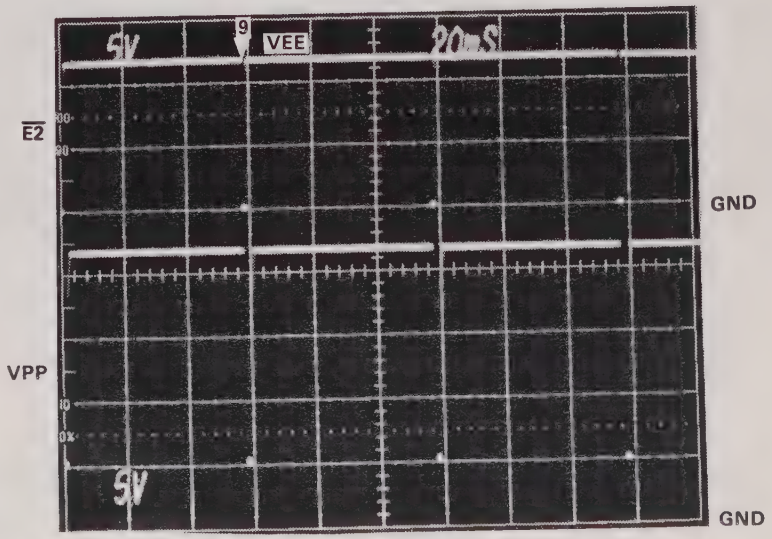
5


5V
20mS
500uS
A0
GND
5V
0555mS
GND

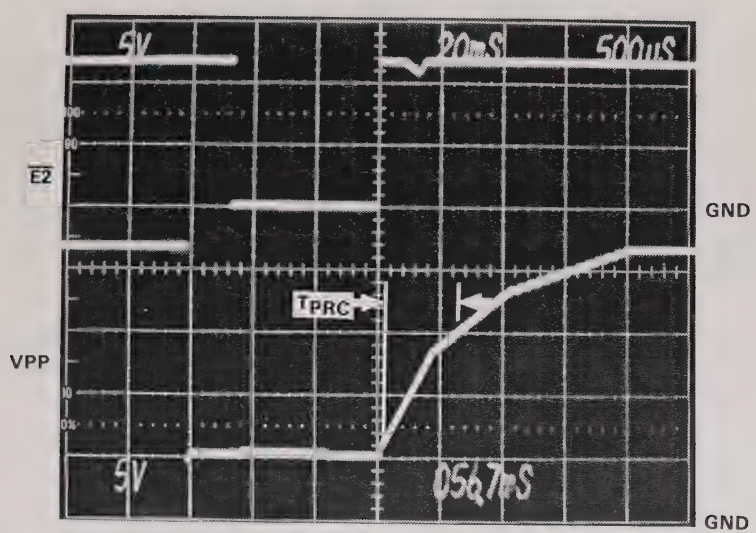
6


20mS
5uS
TF
VPP
5V
1150mS
GND

7


5V
9
VEE
20mS
E2
GND
VPP
5V
GND

8



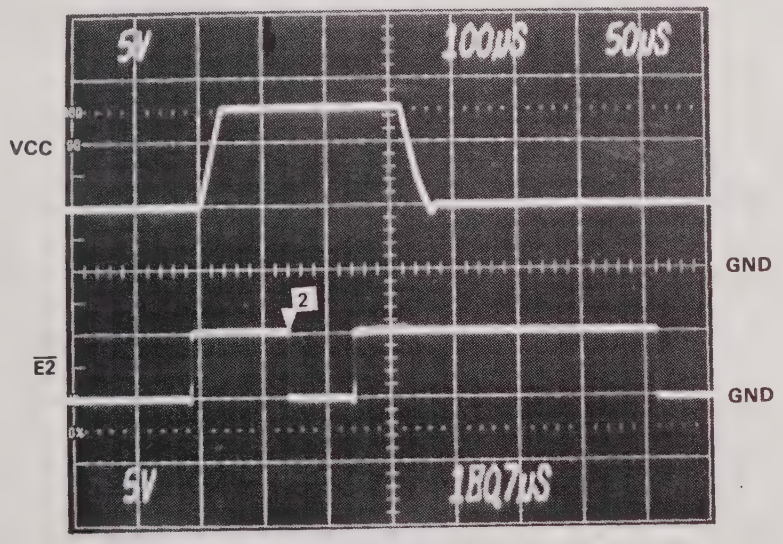
9

10-950-0059

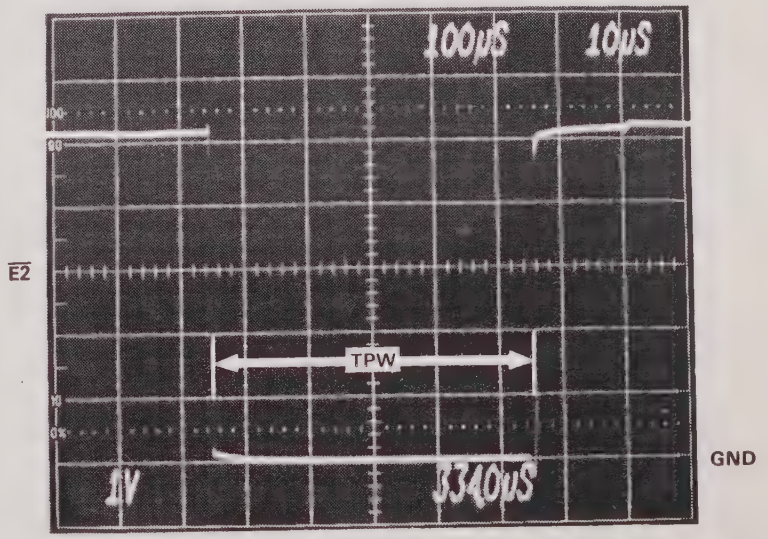
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		E.J.Z.	11/82
	C	ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

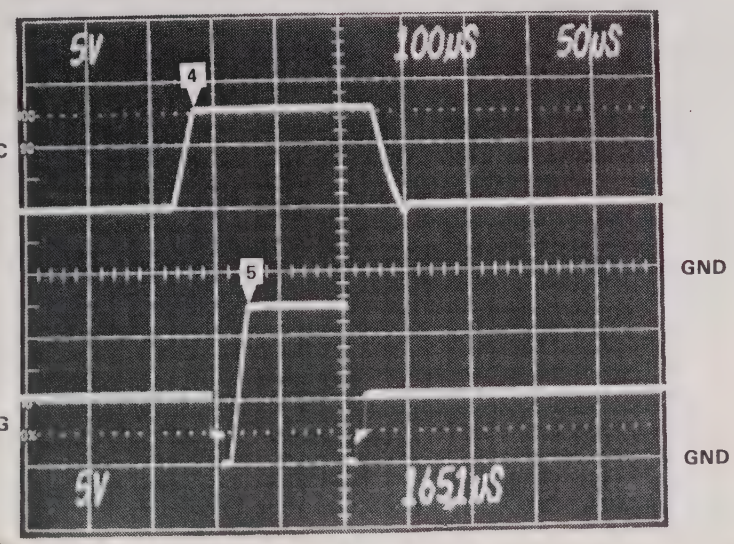
TITLE: TIMING DIAGRAM			DRAWN BY:
FAMILY CODES 85, 86			CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2



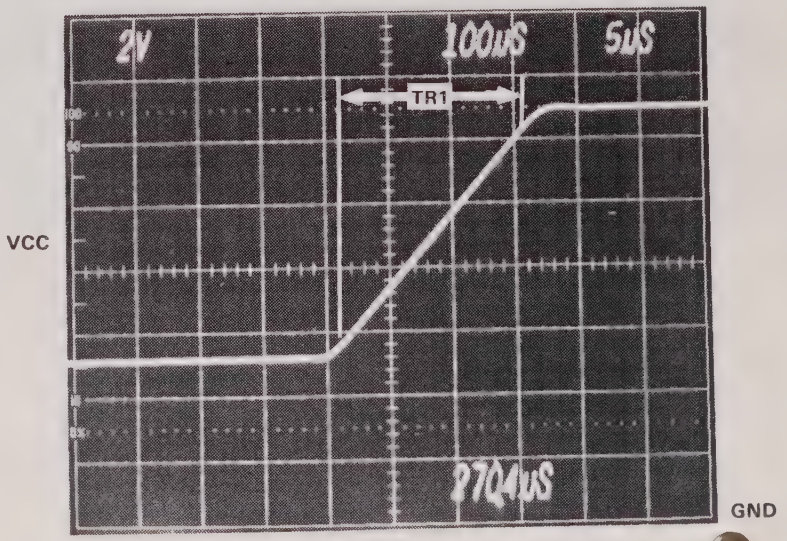
1



2



3



4

10-960-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12.5	12.5	13.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	11.5	12.0	12.5	V	
	TPW	40	50	60	µs	
	TR1	5		20	µs	
	TR2	10		20	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.4	0.5	0.6	V	701-1655/TP2
	High Load	18.0	18.5	19.0	V	701-1655/TP4
	Low Load	18.0	18.5	19.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	High Load	6.0	7.0	8.0	V	701-1655/TP4
	Low Load	6.0	7.0	8.0	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 91.*
2. *Load RAM with $01 for Family 92.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.F.3.	11/82
	C	ECN #4831		JCH	5/85

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 91, 92

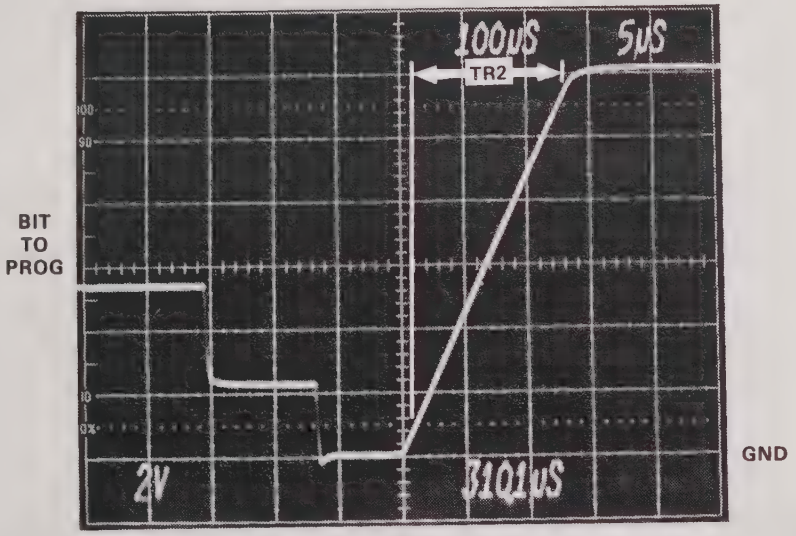
DRAWN BY:

CHECKED BY:

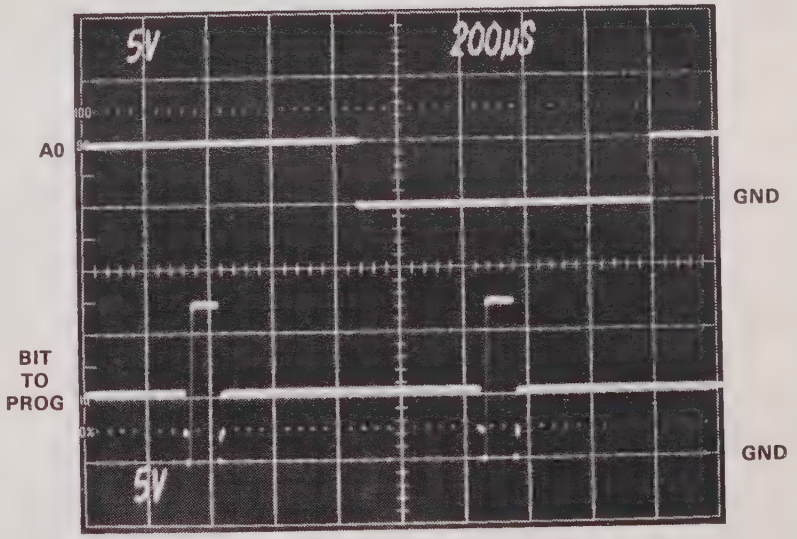
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


100uS
5uS
TR2
BIT
TO
PROG
GND
2V
3101uS

5


5V
200uS
A0
GND
BIT
TO
PROG
GND
5V

6

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.J.Z.	11/82
	C	ECN #4831		[illegible]	5/8[illegible]

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 91, 92

DRAWN BY: [illegible]

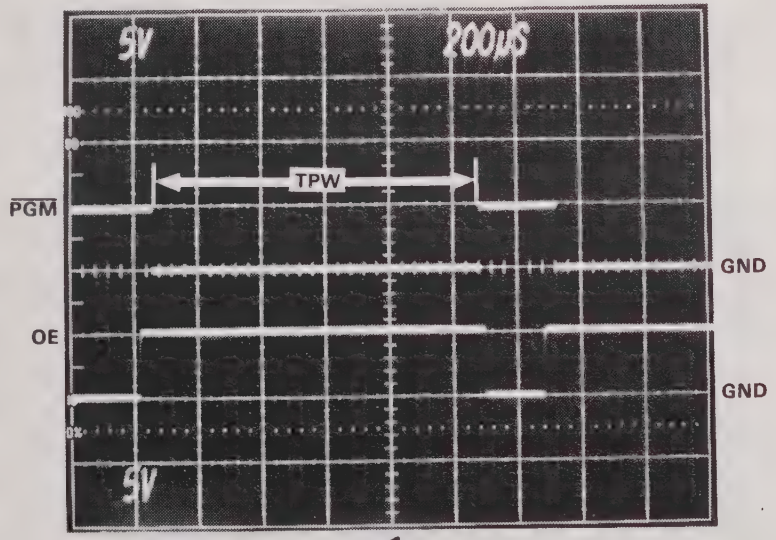
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

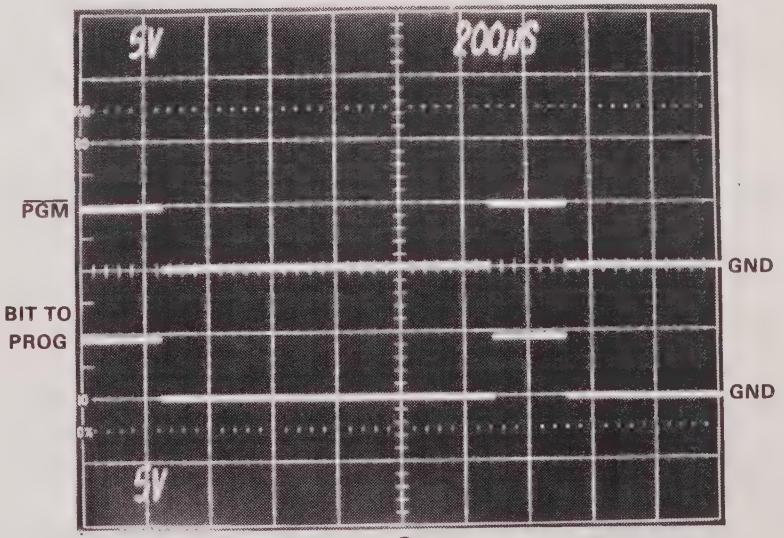
SCALE

SHEET 2/2

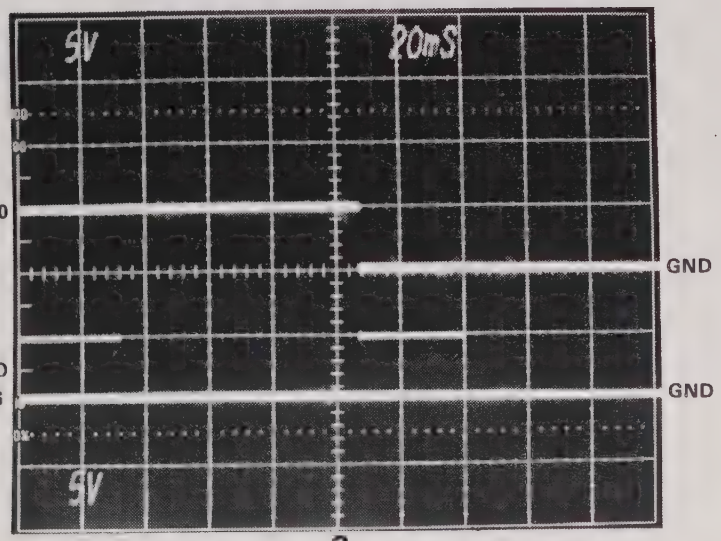
10-950-0059



1



2



3

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	12.2	12.5	12.8	V	Not shown
	VPPV					NA
	TPW	.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		25		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family 93.*
2. *Load RAM with $01 for Family 94, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 3 ms times the number of programming pulses required to program the location.*

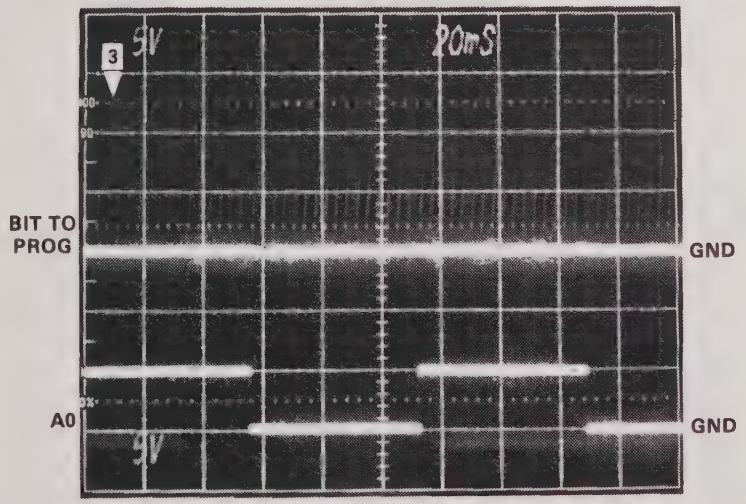
10-950-0059

REVISIONS

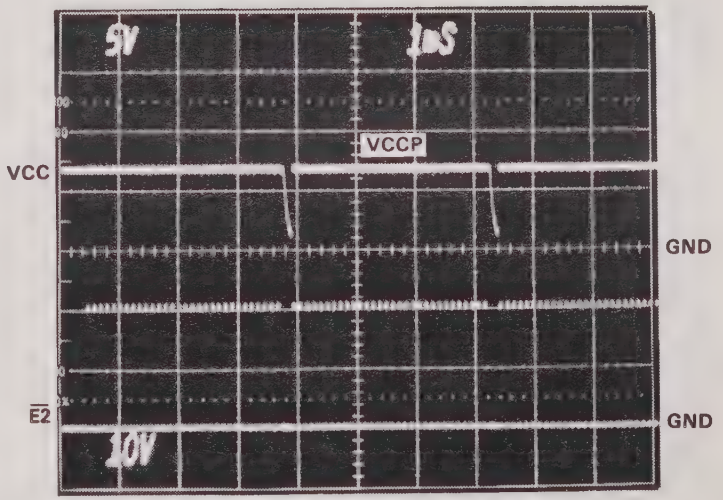
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		XH	5/83

DATA I/O

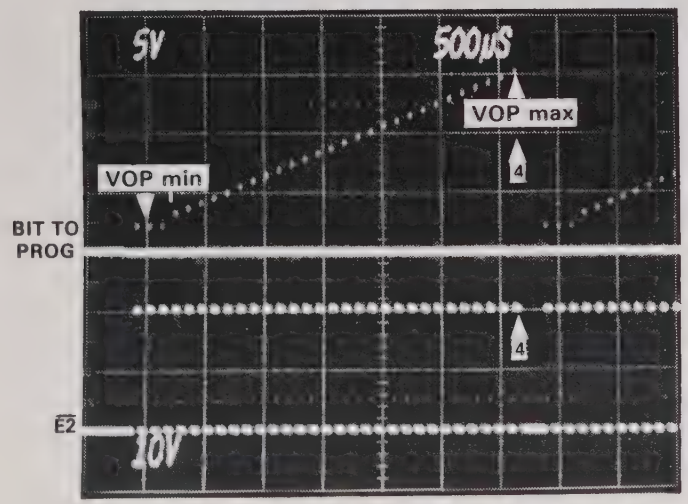
TITLE: TIMING DIAGRAM FAMILY CODES 93, 94		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE:		SHEET 1 of 1


5V
20mS
3
BIT TO PROG
GND
A0
GND
5V

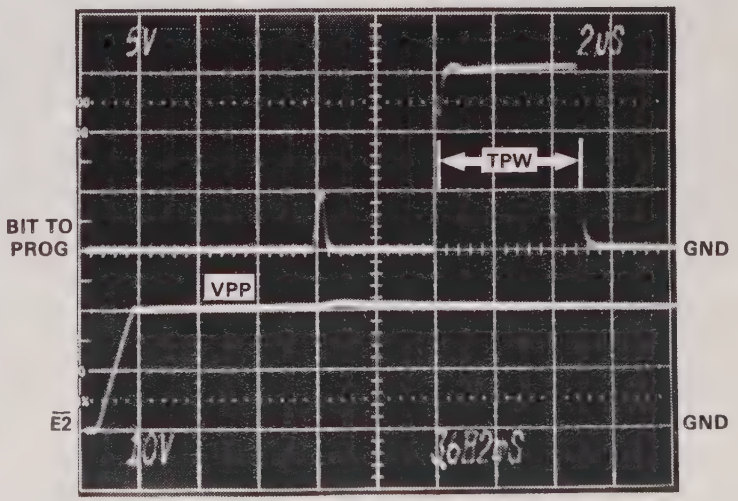
1


5V
1mS
VCCP
VCC
GND
E2
GND
10V

2


5V
500µS
VOP max
VOP min
4
BIT TO PROG
4
E2
10V

3


5V
2uS
TPW
BIT TO PROG
GND
VPP
E2
GND
10V
6.82mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	6.3	6.5	6.7	V	
	VPP	19.5	20.0	20.5	V	
	VOP max	15.5	16.0	16.5	V	See note 2
	VOP min	1.5	2.0	2.5	V	See note 2
	TPW	4.0	5.0	6.0	us	
	Reject		16		Series	See note 3
	Overprogram		1		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	17.2	18.2	19.2	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	17.2	18.2	19.2	V	701-1655/TP3

NOTES

1A. Fill RAM with $FE for Family A3.
1B. Fill RAM with $01 for Family A4.
2. O1 is loaded with a 100Ω resistor. A series of program pulses is applied. The program pulses begin at VOP min and increase in magnitude to VOP max or until the bit programs.
3. Reject count is 16 program pulse series.

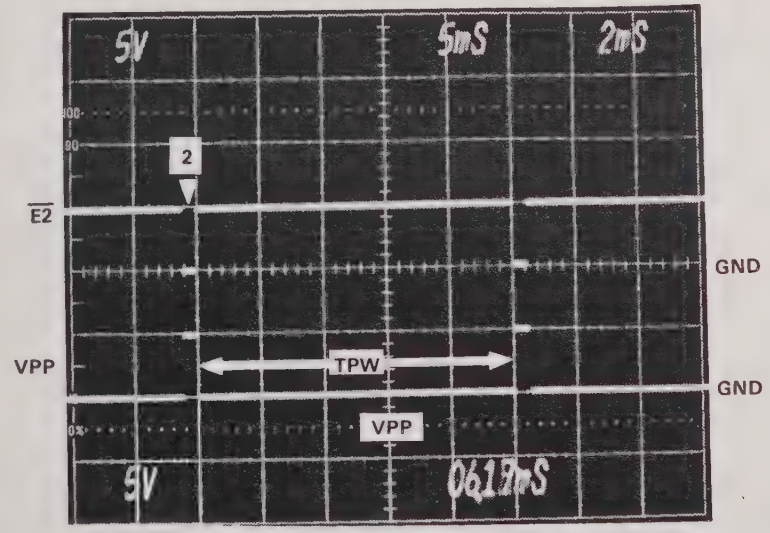
10-950-0059

REVISIONS

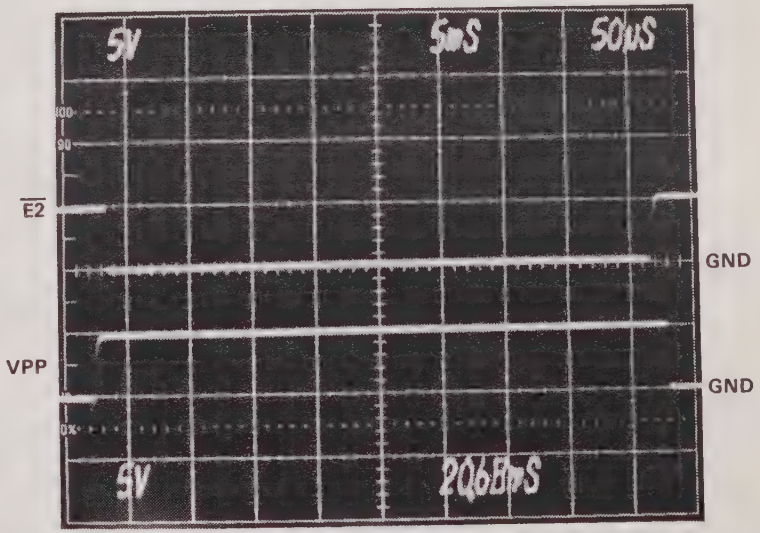
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		JCH	5 21

DATA I/O

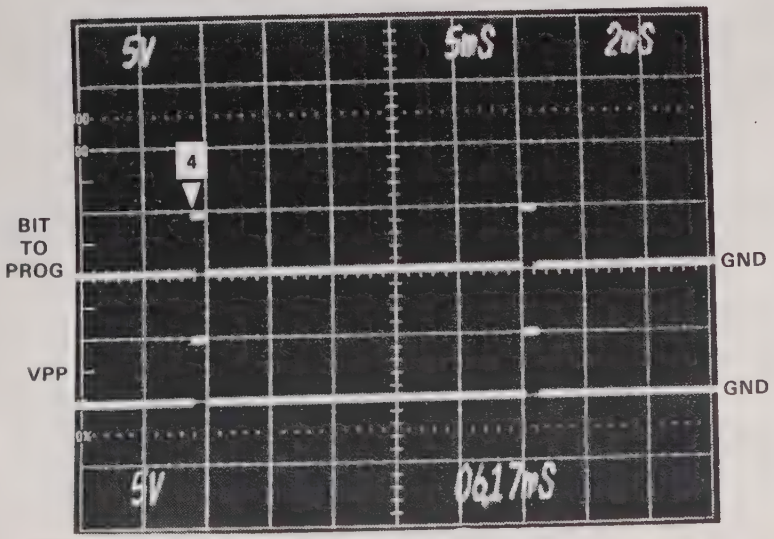
TITLE: TIMING DIAGRAM FAMILY CODES A3, A4		DRAWN BY:
		CHECKED BY: RH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE:		SHEET 1 of 1



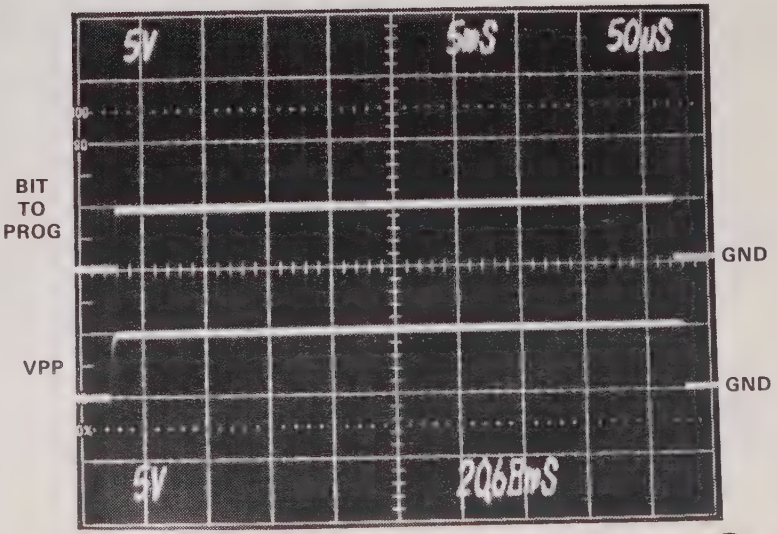
1



2



3



4

10-960-059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.5	5.0	5.5	V	
	VPP	0.0	0.0	0.8	V	
	VEE	12.0	14.5	21.0	V	
	TPW	5.0	10.0	15.0	ms	
	TR				NA	
	TF				NA	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	.4	.5	.6	V	701-1655/TP2
	High Load	4.5	5.5	6.5	V	701-1655/TP4
	Low Load	4.5	5.5	6.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	High Load	0.0	0.0	.4	V	701-1655/TP4
	Low Load	6.8	7.8	8.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family A5.*
2. *Load RAM with $01 for Family A6, and Bit-to-Prog waveform becomes Bit-no-Prog waveform.*
3. *Photos 6 and 7 are erase waveforms.*

10-960-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.S.3.	11/82
	C	ECN #4831		JH	3/83

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES A5, A6

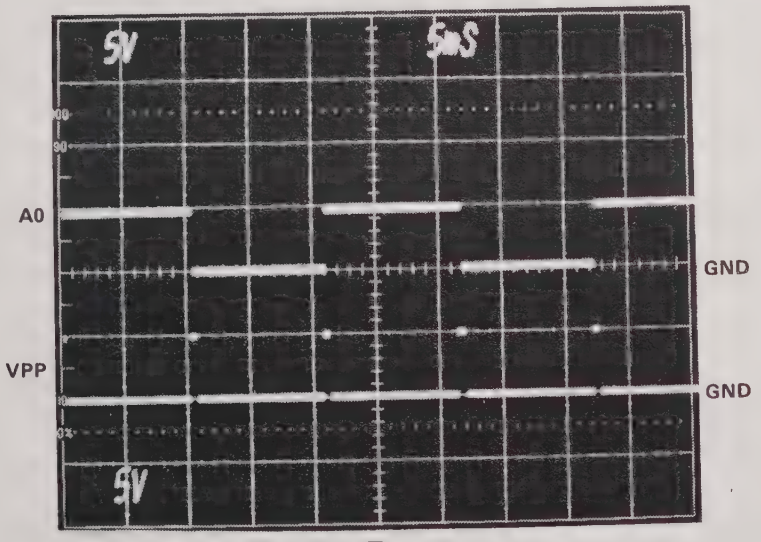
DRAWN BY:

CHECKED BY: JH

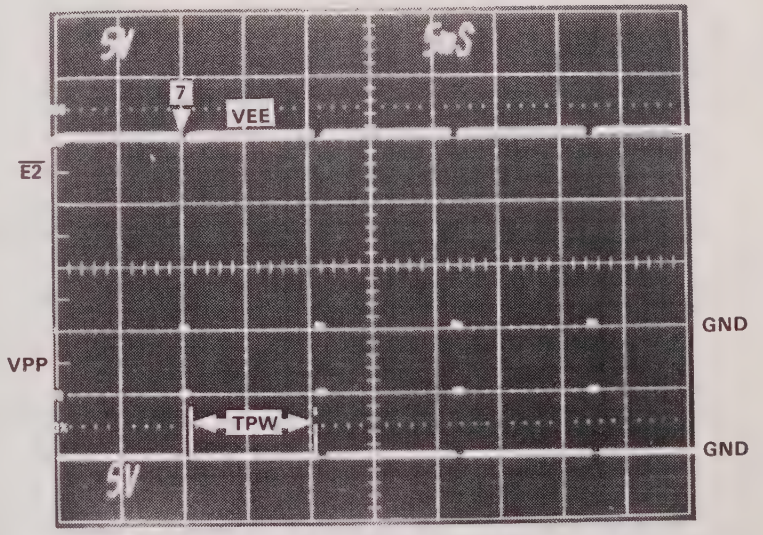
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

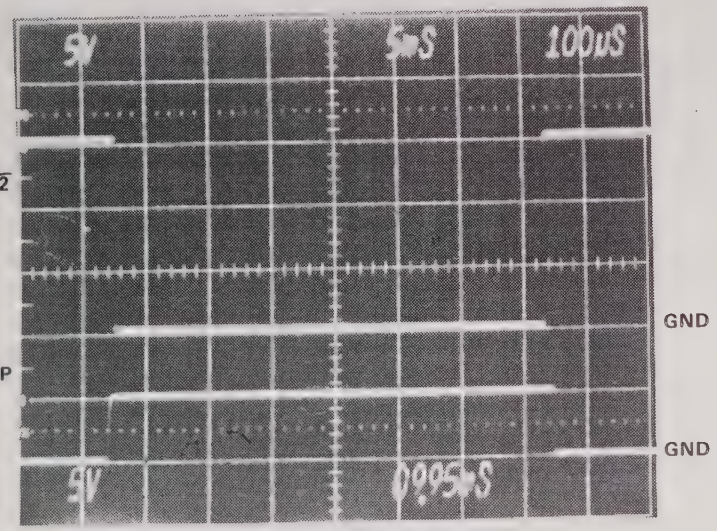
SHEET 1/2


5V
5mS
A0
GND
VPP
GND
5V

5


5V
5mS
7
VEE
E2
GND
VPP
TPW
GND
5V

6

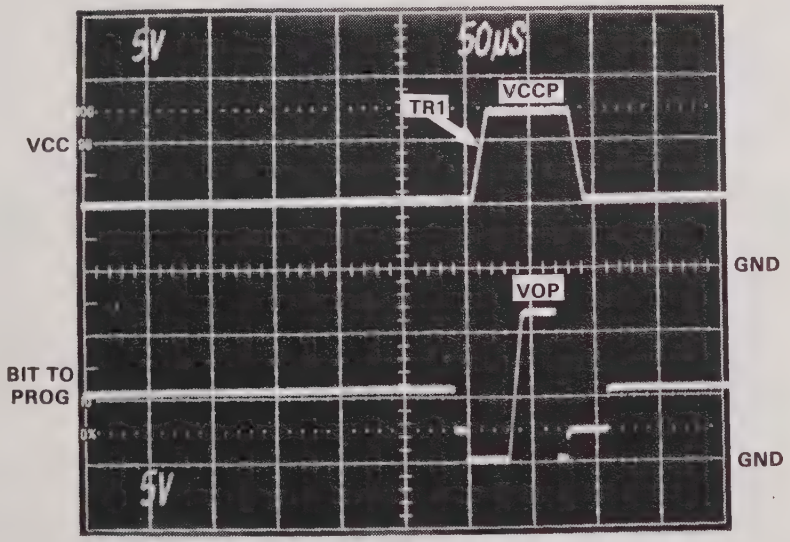

5V
5mS
100uS
E2
GND
VPP
GND
5V
0.005mS

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release		C.T.J.	11/82
	C	ECN #4831		XX	5/83

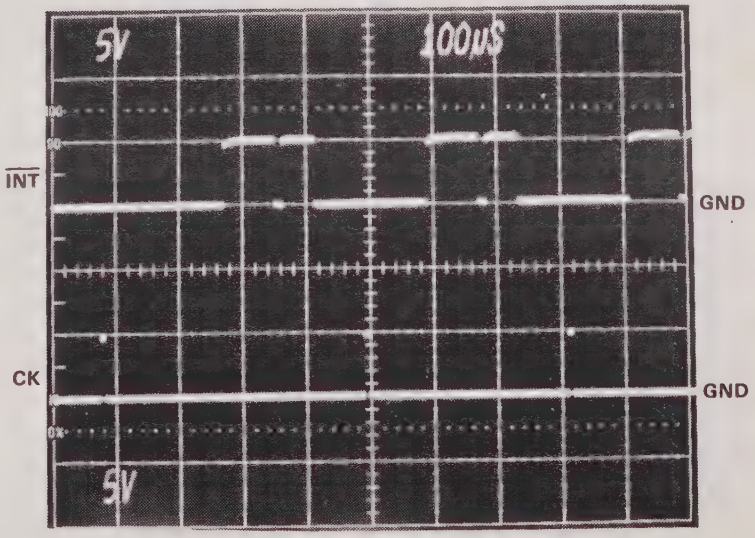
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM		DRAWN BY:
FAMILY CODES A5, A6		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

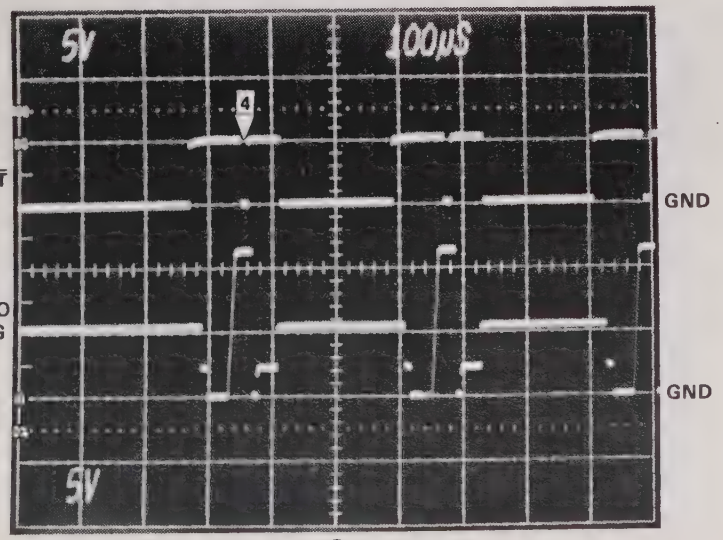
10-950-0059


5V
50µS
TR1
VCCP
VCC
GND
VOP
BIT TO PROG
GND
5V

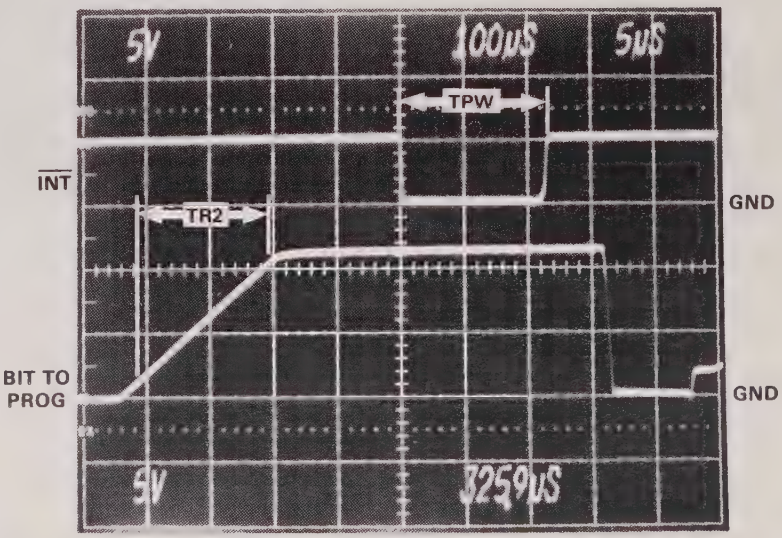
1


5V
100µS
INT
GND
CK
GND
5V

2


5V
100µS
4
INT
GND
BIT TO PROG
GND
5V

3


5V
100µS
5uS
TPW
INT
TR2
GND
BIT TO PROG
GND
5V
3259µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.6	11.8	12.0	V	
	VOP	10.5	11.0	11.5	V	
	VPP					NA
	VPPV					NA
	TPW	9.0	10.0	11.5	us	
	TR1	1.0		20.0	us	See note 3
	TR2	1.0		15.0	us	
	TF					NA
	Reject		10		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.6	8.1	8.6	V	701-1655/TP4
	Low Load	7.6	8.1	8.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	8.8	9.3	9.8	V	701-1655/TP4
	Low Load	8.8	9.3	9.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family A9.*
2. *Load RAM with $01 for Family AA.*
3. *Load VCC with a 330 , ½ W resistor.*

10-960-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		YH	5/83

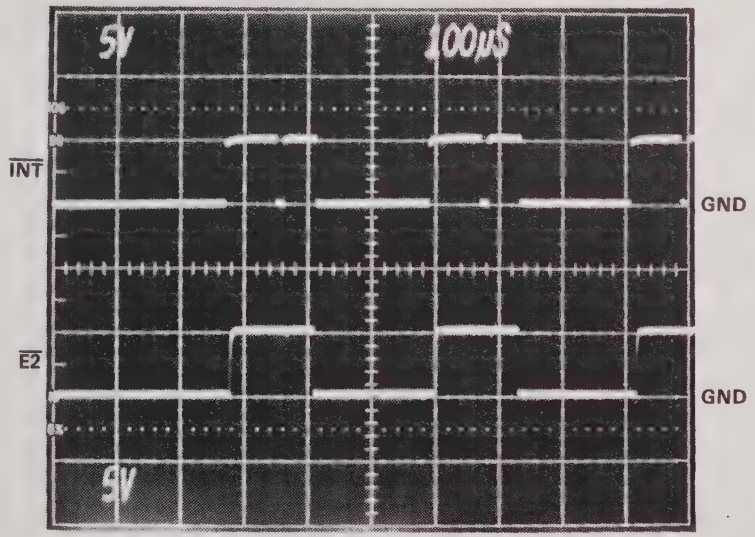
DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODES A9, AA

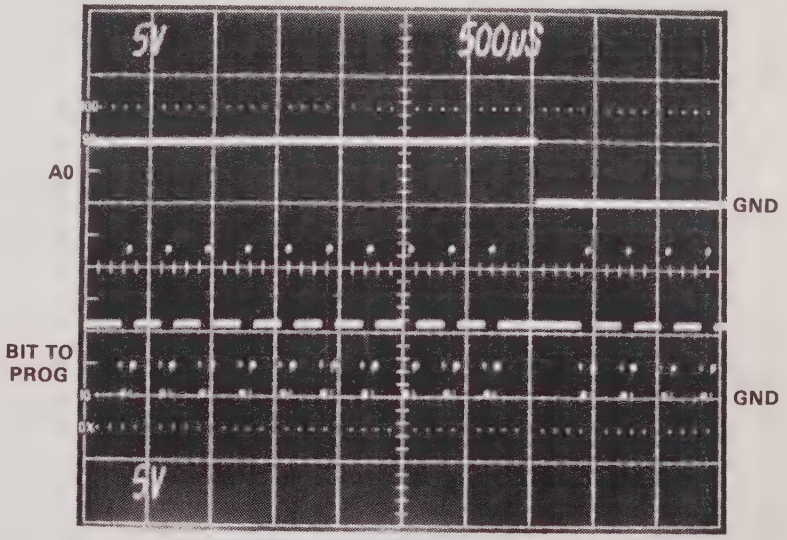
DRAWN BY:

CHECKED BY: YH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059



5



6

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		[illegible]	[illegible]

DATA I/O

TITLE

TIMING DIAGRAM

FAMILY CODES A9, AA

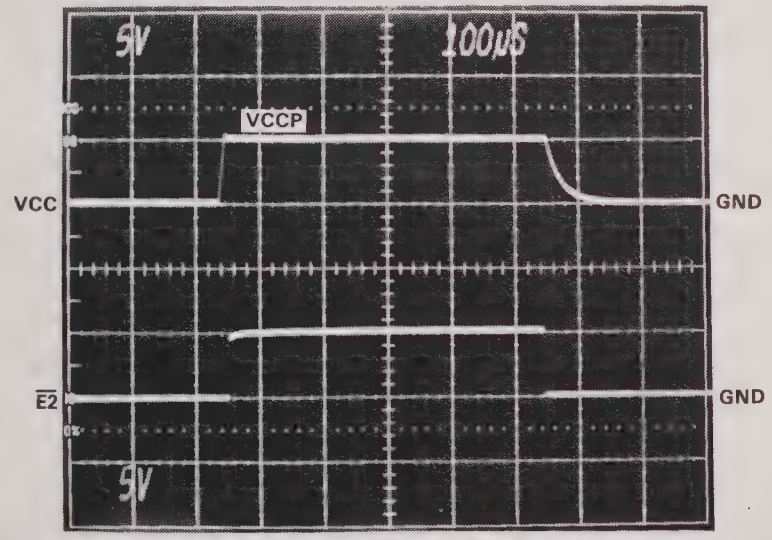
DRAWN BY:

CHECKED BY:

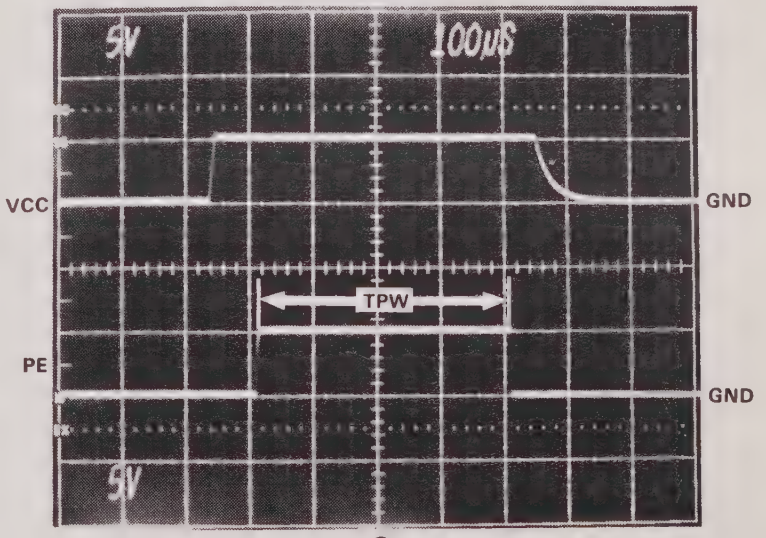
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

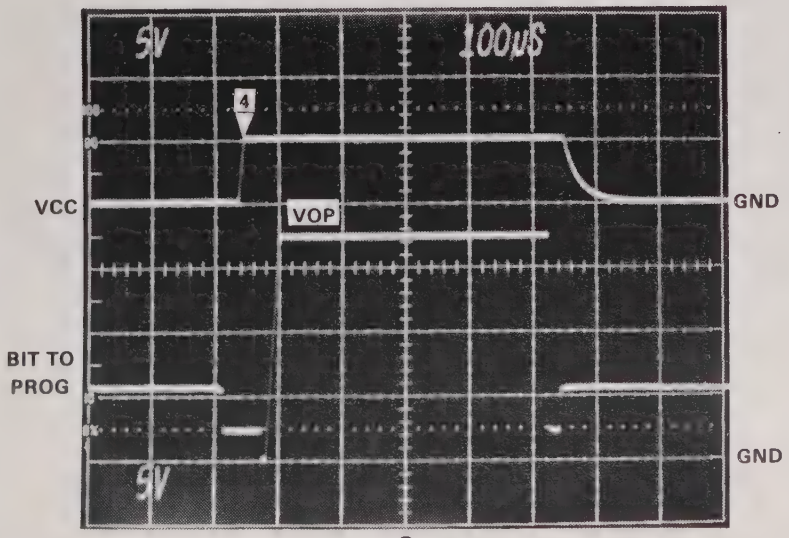
SHEET



1



2



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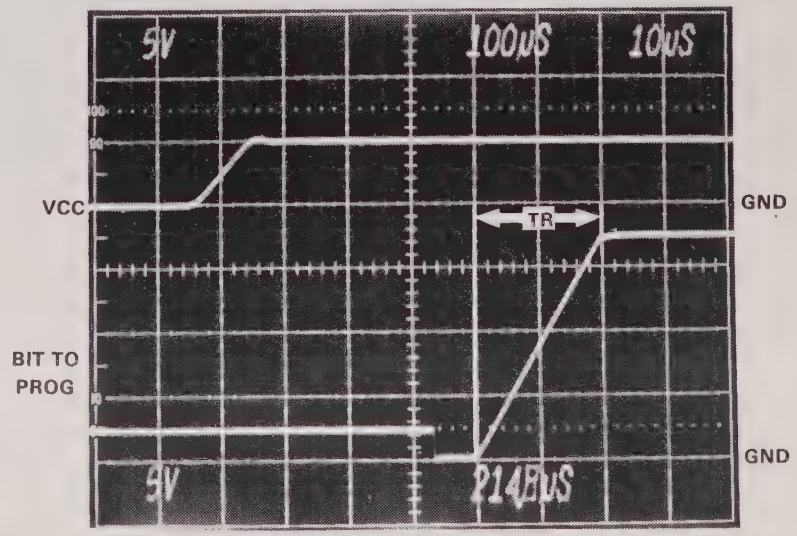


4

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	
	VOP	16.0	17.0	18.0	V	
	VPP					NA
	VPPV					NA
	TPW	300	400	500	us	
	TR	10		50	us	
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family AD.*
2. *Load RAM with $01 for Family AE.*

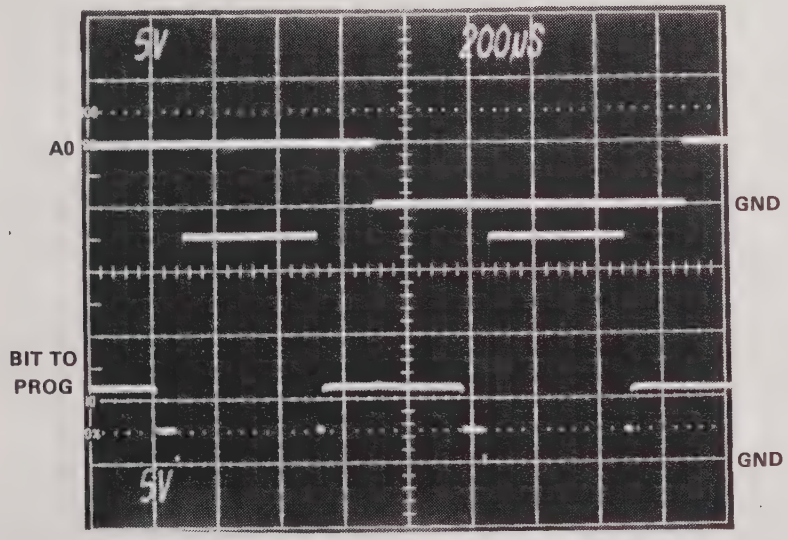
6500-056-01

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		XH	5/83

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES AD, AE	DRAWN BY: CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	



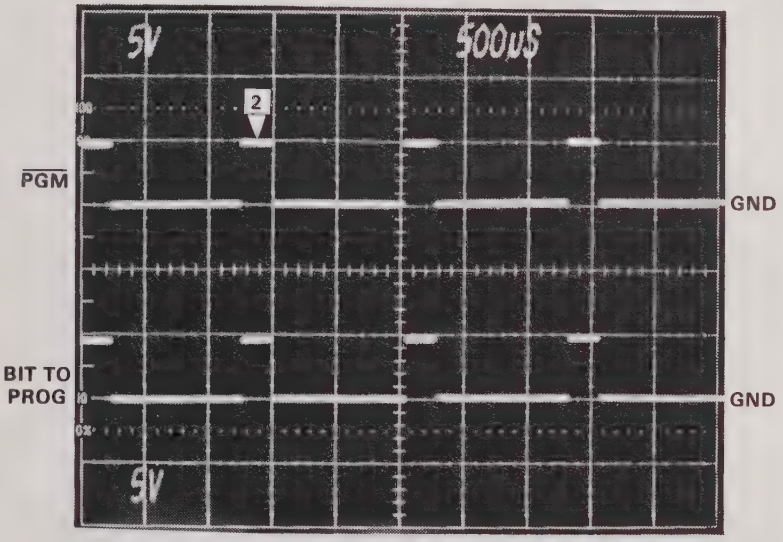
5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		XH	5/83

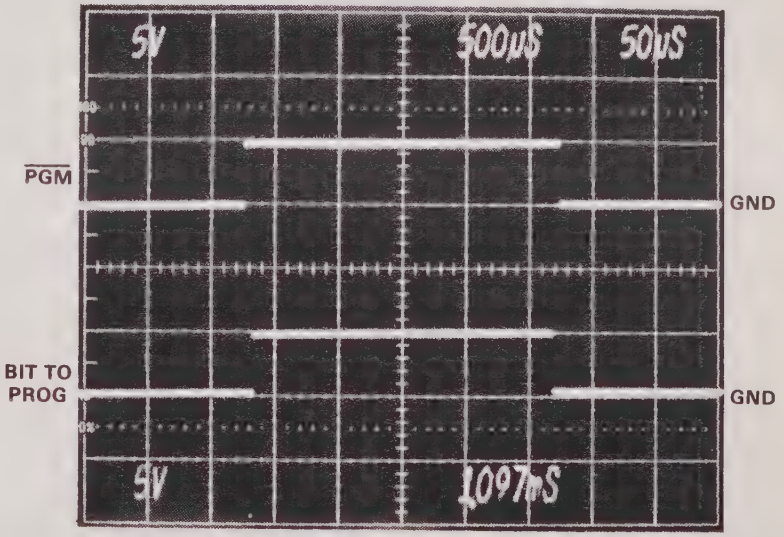
DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES AD, AE		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2

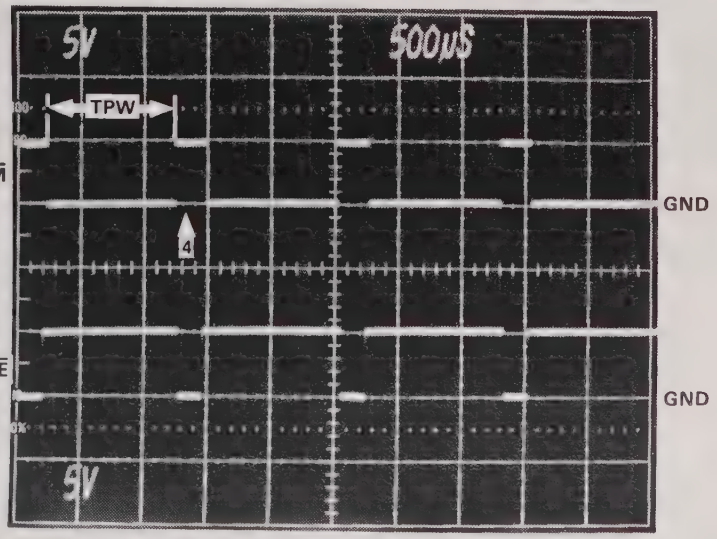
10-950-0059



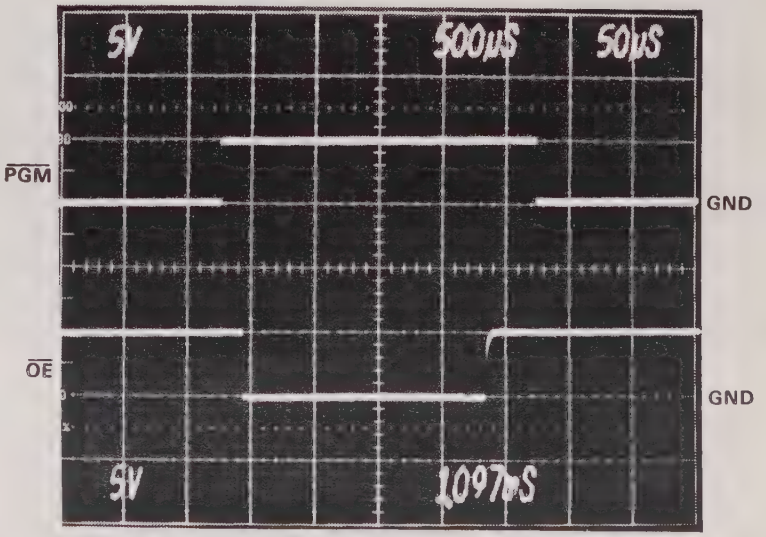
1



2



3



4

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	Not shown
	VOP					NA
	VPP	21.0	21.5	22.0	V	Not shown
	VPPV					NA
	TPW	.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		40		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS	VCC	5.5	5.6	5.7	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family AF.*
2. *Load RAM with $01 for Family B0 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 4 ms long; see photo 6, 7.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		XH	5/83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODES AF, B0

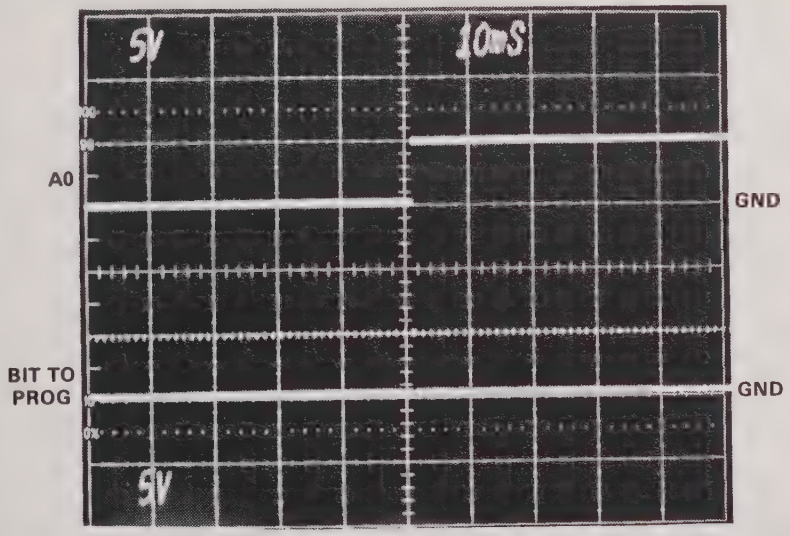
DRAWN BY:

CHECKED BY: XH

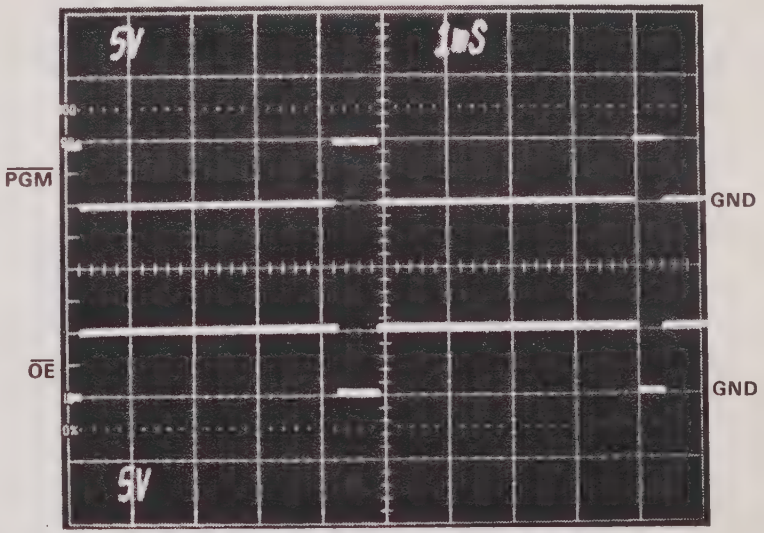
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

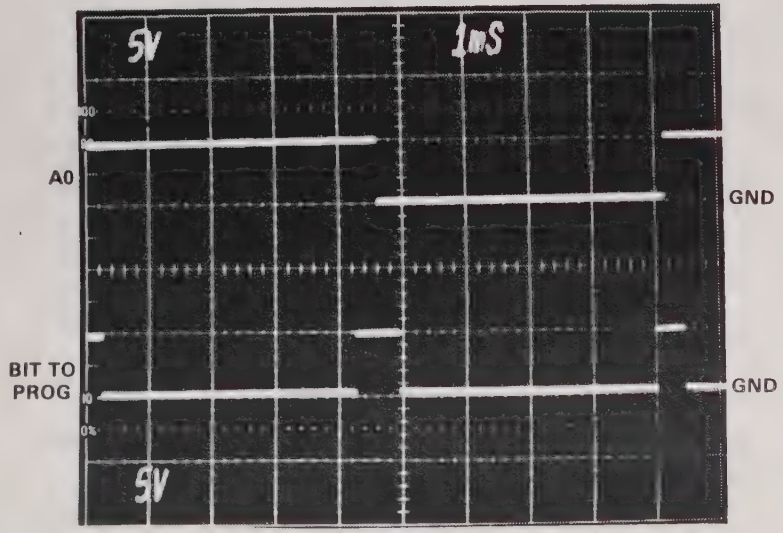
SHEET 1 of 2


5V
10mS
A0
GND
BIT TO PROG
GND
5V

5


5V
1mS
PGM
GND
OE
GND
5V

6


5V
1mS
A0
GND
BIT TO PROG
GND
5V

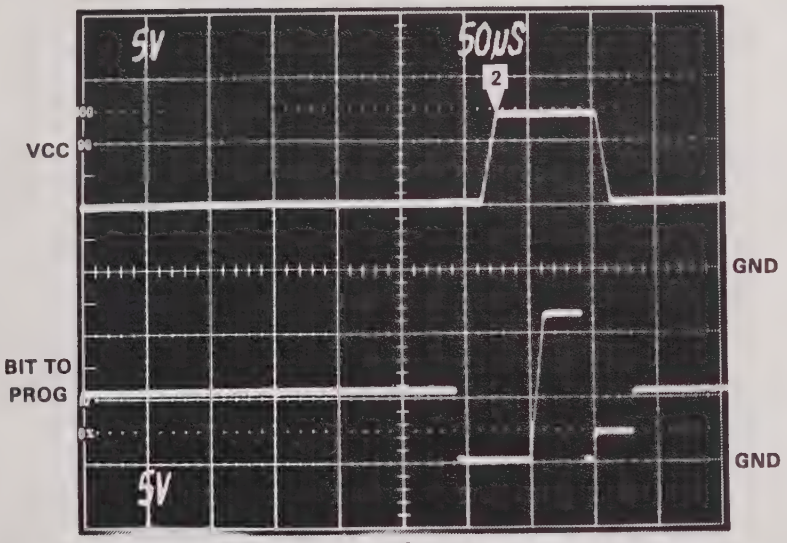
7

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	Release			
	C	ECN #4831		J-H	5/6

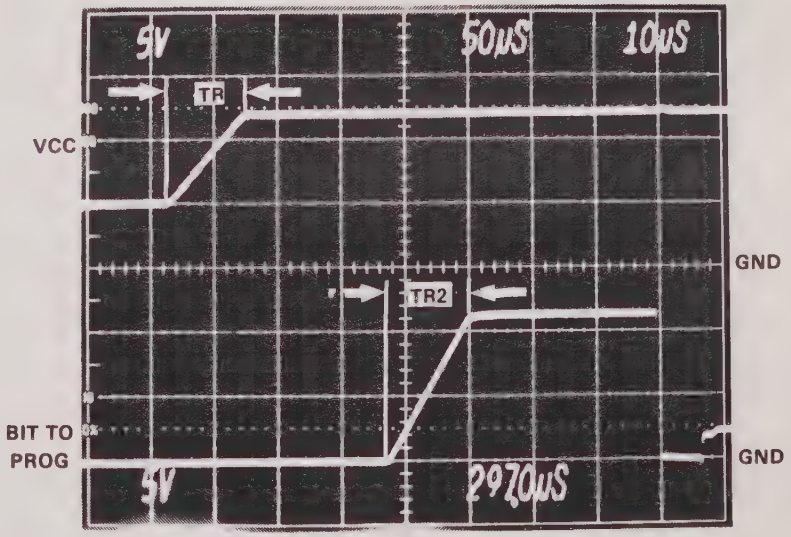
DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES AF, BO		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2

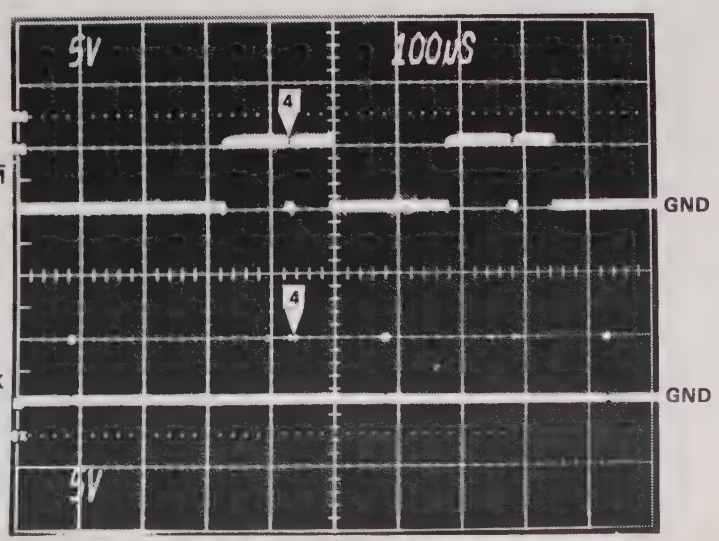
10-950-0059



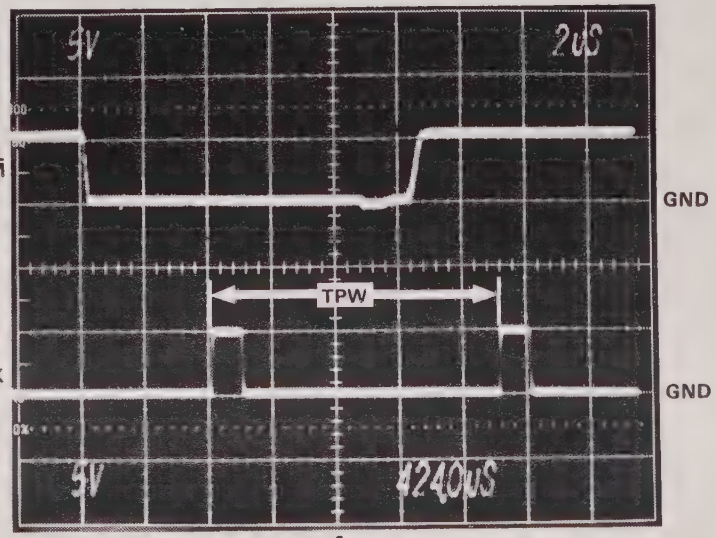
1



2



3



4

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.6	11.8	12.0	V	
	VOP	10.5	11.0	11.5	V	
	VPP					NA
	VPPV					NA
	TPW	9.0	10.0	11.5	us	
	TR1	1.0		20.0	us	See note 3
	TR2	1.0		15.0	us	
	TF					NA
	Reject		10		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.6	8.1	8.6	V	701-1655/TP4
	Low Load	7.6	8.1	8.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	8.8	9.3	9.8	V	701-1655/TP4
	Low Load	8.8	9.3	9.8	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family B1.*
2. *Load RAM with $01 for Family B2.*
3. *Load VCC with a 330Ω , ½W resistor.*

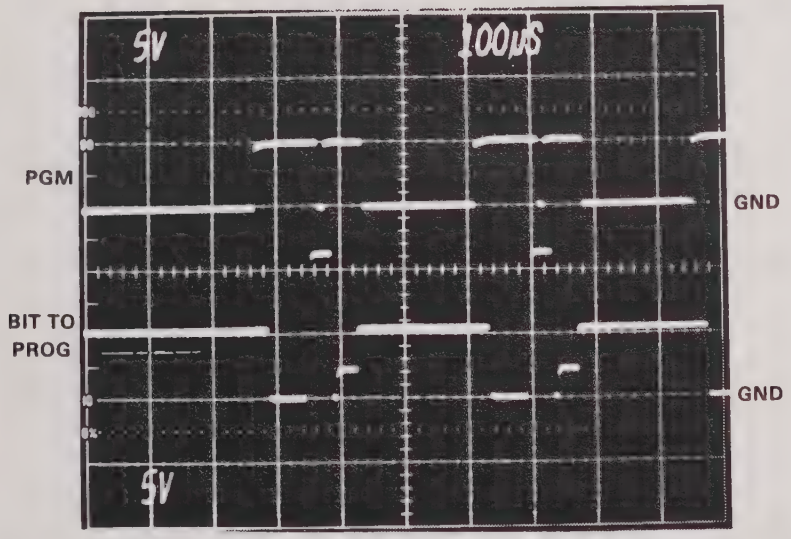
10-950-0059

REVISIONS

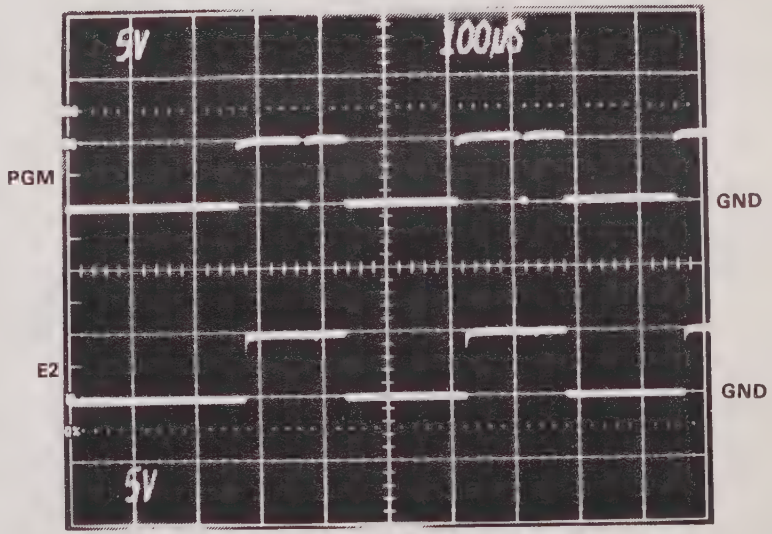
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		XH	5/83

DATA I/O

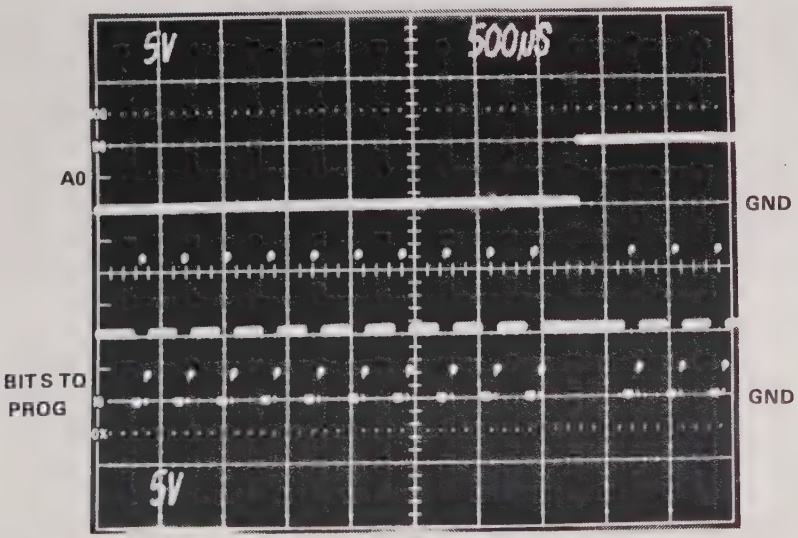
TITLE: TIMING DIAGRAM FAMILY CODES B1, B2		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
100µS
PGM
GND
BIT TO
PROG
GND
5V

5


5V
100µS
PGM
GND
E2
GND
5V

6


5V
500µS
A0
GND
BIT S TO
PROG
GND
5V

7

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		XH	5/83

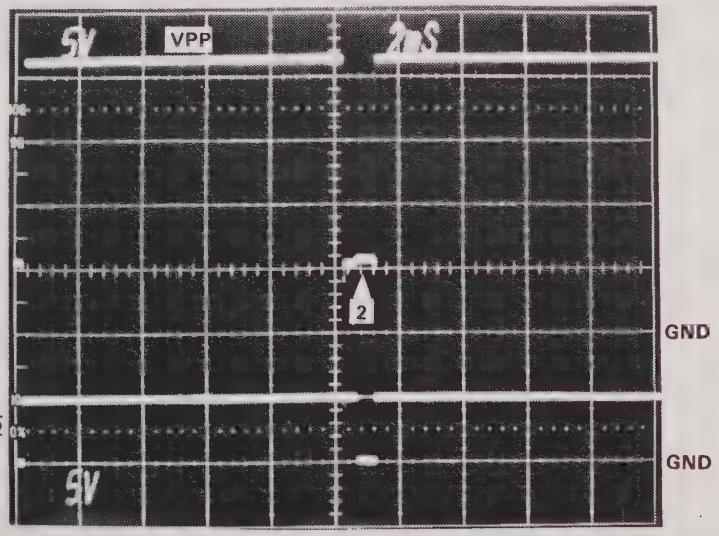
DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES B1, B2	DRAWN BY:
	CHECKED BY: XH

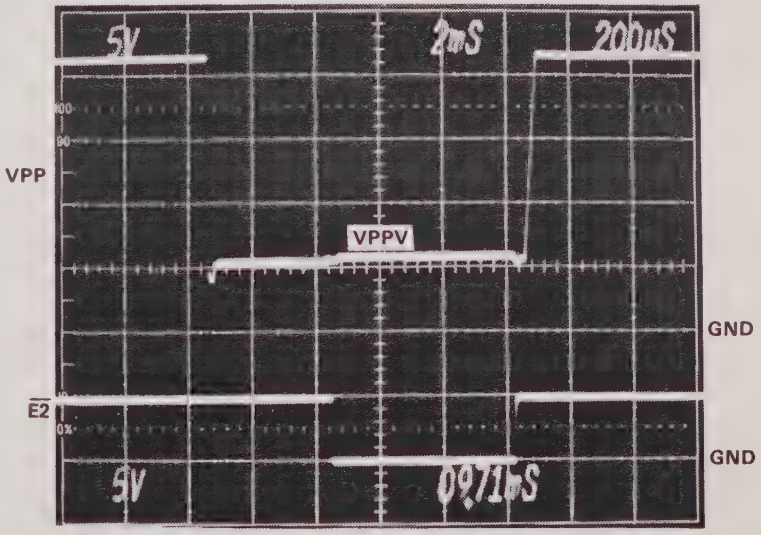
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 2 of 2

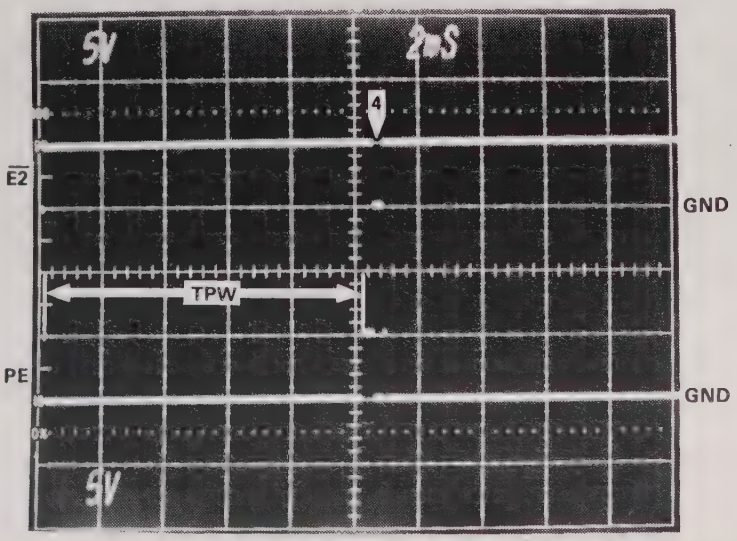
10-950-0059


5V
VPP
2mS
VPP
2
GND
E2
GND
5V

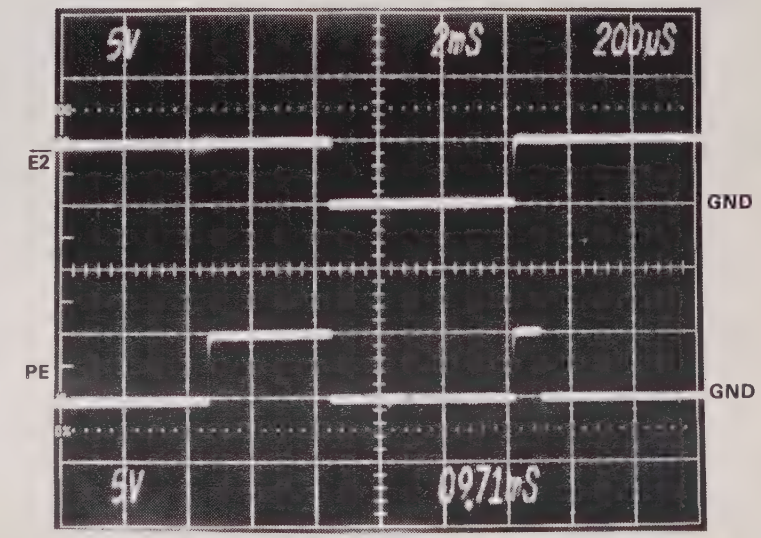
1


5V
2mS
200uS
VPP
VPPV
GND
E2
GND
5V
09.71mS

2


5V
2mS
4
E2
GND
TPW
PE
GND
5V

3


5V
2mS
200uS
E2
GND
PE
GND
5V
09.71mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	VEE	9.0	12.0	15.0	V	
	TPW	9.0		15.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family B3.*
2. *Load RAM with $01 for Family B4 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Chip erase waveforms are photos 8 and 9.*
4. *Byte erase waveforms are photos 10 and 11.*

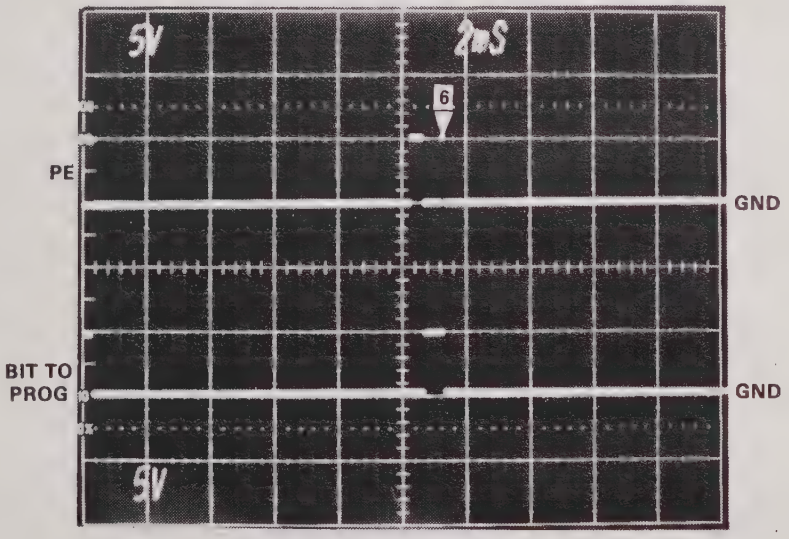
10-950-0059

REVISIONS

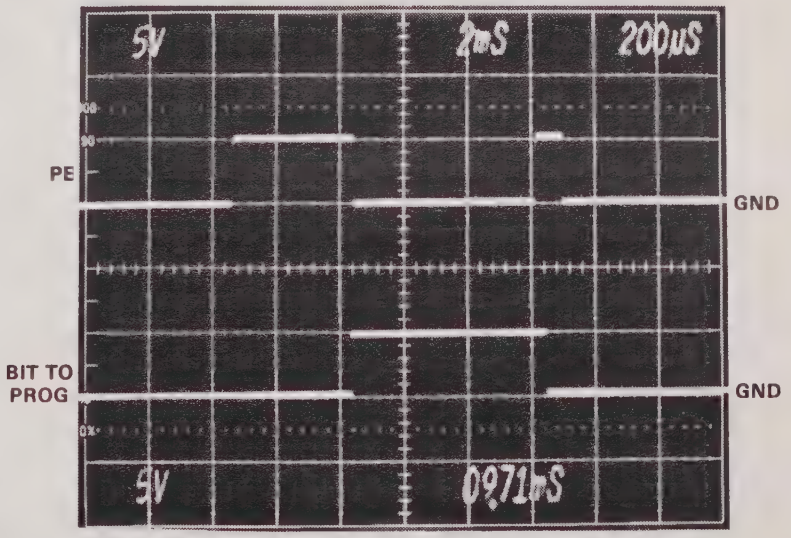
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		JCH	5/83

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES B3, B4			DRAWN BY:
			CHECKED BY: JH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 1 of 3


5V
2mS
6
PE
GND
BIT TO
PROG
GND
5V

5


5V
2mS
200uS
PE
GND
BIT TO
PROG
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5V
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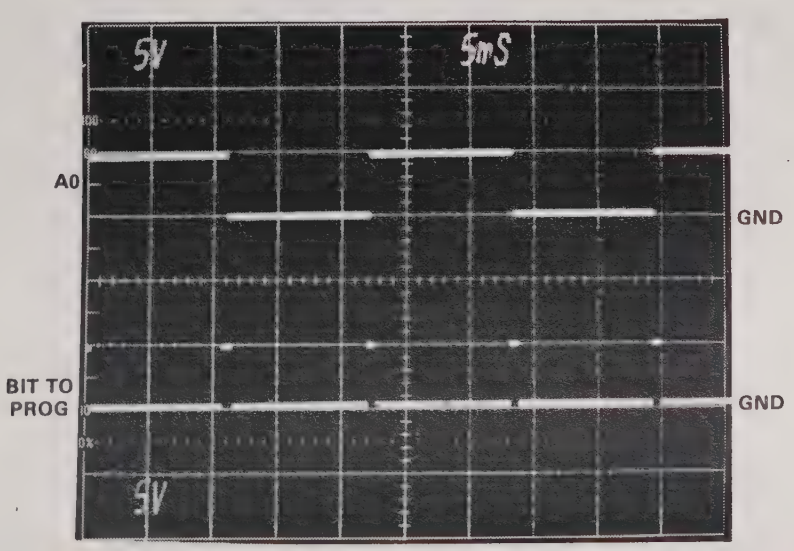
6


5V
5mS
A0
GND
BIT TO
PROG
GND
5V

7

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831			

DATA I/O

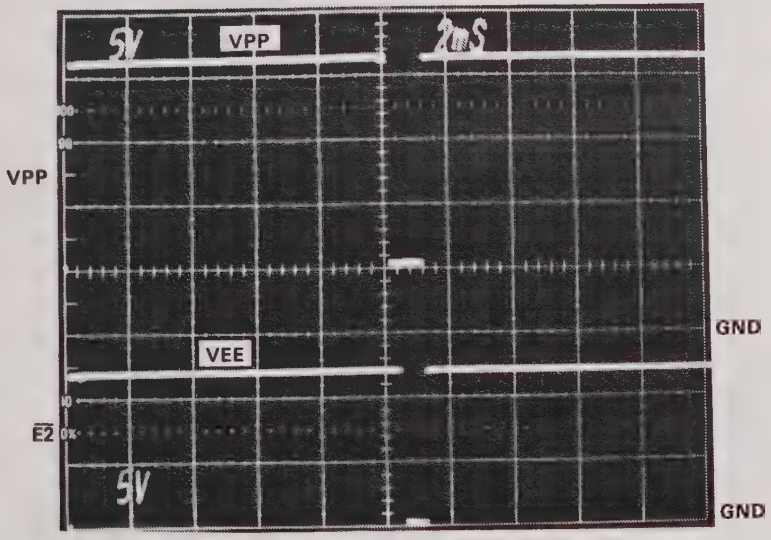
TITLE
TIMING DIAGRAM
FAMILY CODES B3, B4

DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE



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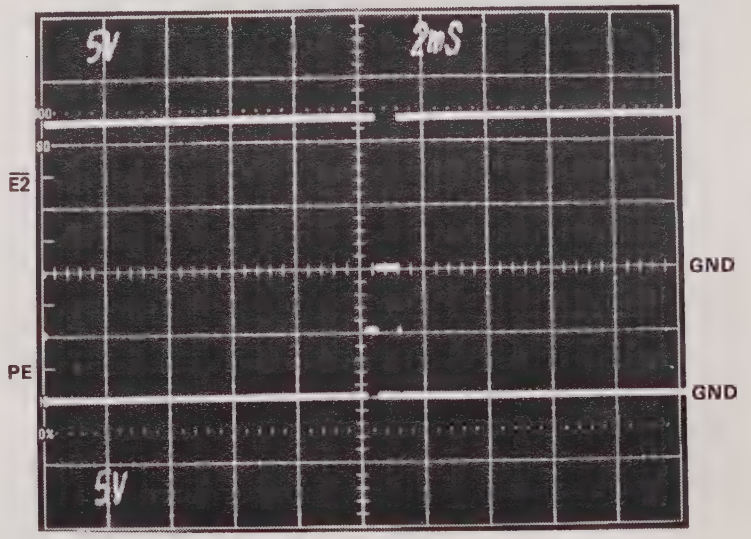

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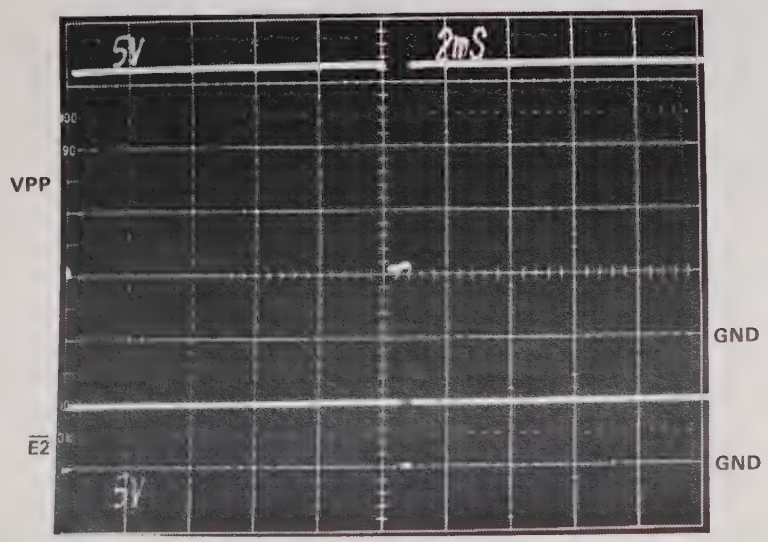

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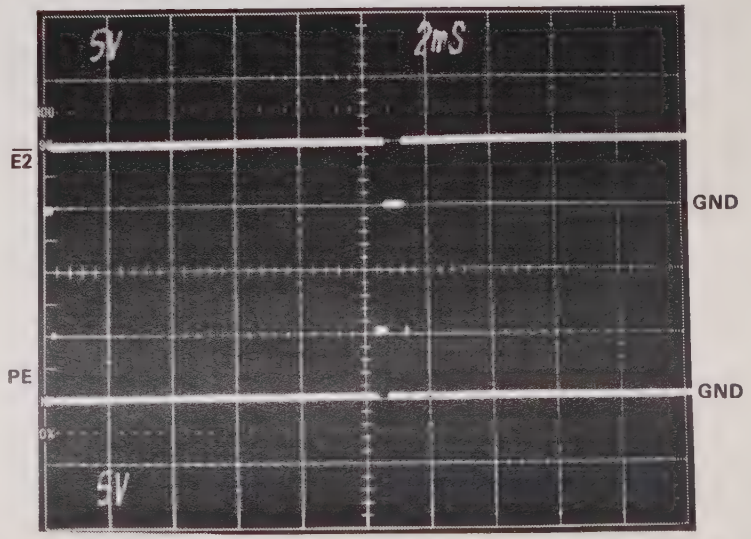


11

10-950-0059

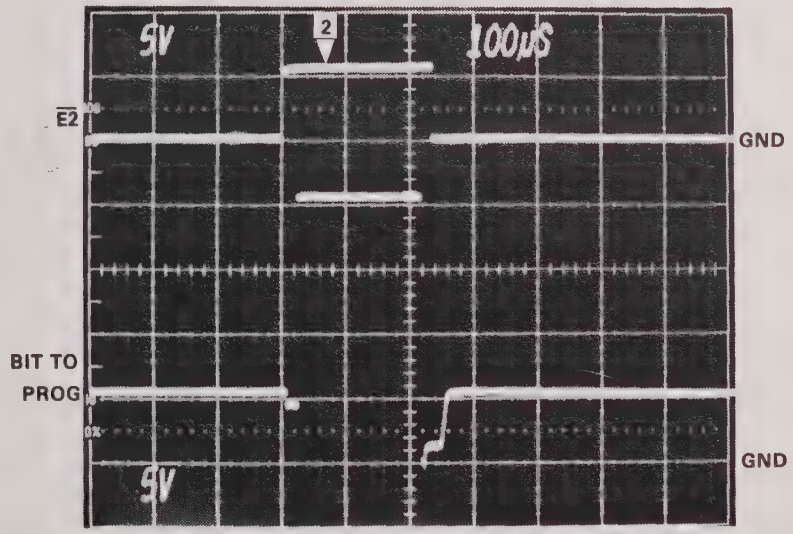
10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831		XH	5/83

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES B3, B4		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3 of 3



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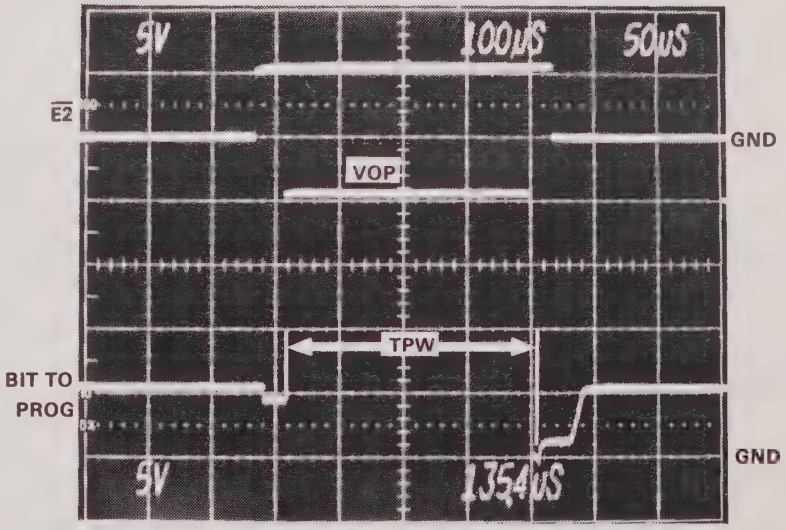

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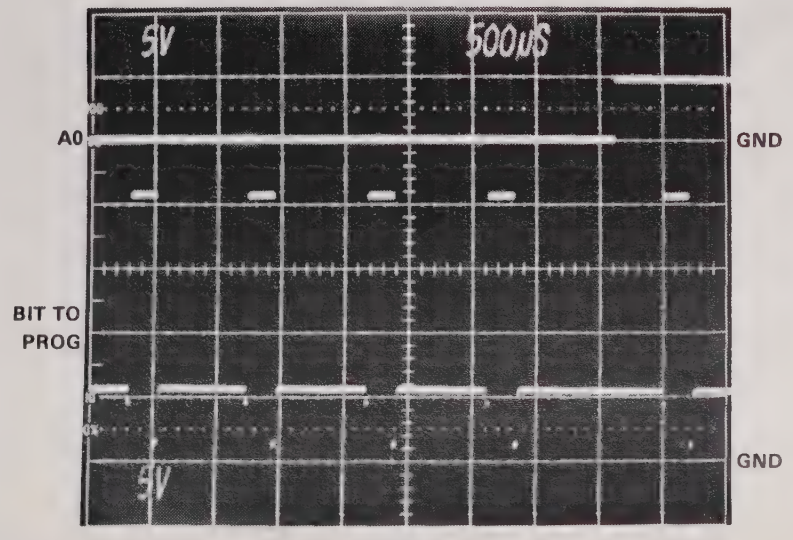

3

10-960-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not shown
	VOP	20.0	20.5	21.0	V	
	VPP					NA
	VPPV					NA
	TPW	180	190	200	us	At 10V Level
	TR					NA
	TF					NA
	Reject		4		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.3	4.4	4.5	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	24.8	25.3	25.8	V	701-1655/TP4
	Low Load	24.8	25.3	25.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	6.3	6.8	7.3	V	701-1655/TP4
	Low Load	6.3	6.8	7.3	V	701-1655/TP3

NOTES

1. *Load RAM with $FE for Family B5.*
2. *Load RAM with $01 for Family B6.*

10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4831			

DATA I/O

TITLE: TIMING DIAGRAM

FAMILY CODES B5, B6

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UNIPAK 2/2B™

Software Update Kit

985-0002-006 *MARCH 87*

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Applies to Engineering Part Numbers 953-0002-013 and up and 953-0017-007 and up

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Introduction

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-027	U20
	EPROM	1	324-0059-028	U21
	Decode PROM	1	324-0037-001	U19
	Label	1	—	
	UniPak 2 Operator's Manual	1	981-0001	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-027	U20
	EPROM	1	324-0059-028	U21
	Decode PROM	1	324-0037-001	U19
	Label	1	—	
	UniPak 2B Device List	1	090-0080	
	UniPak 2B Acceptance Test	1	981-0184	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: 5722/V12

CAUTION

The software update kit EPROMs are static sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROM(s) may result.

UniPak 2/2B Software Update Kit Installation

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- IC extractor tool, or small slot-head screwdriver
- Soldering equipment

NOTE

If you are also installing a UniPak 2 to 2B Conversion Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software update kit:

1. *Proceed directly to step 9 of the following subsection, UniPak 2/2B Disassembly.*
2. *Complete the software update kit installation as directed.*
3. *After completing the software update kit installation, proceed to section 3 of the conversion kit manual and complete the conversion kit installation.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free work station.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1a) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1b) to unlock the flanges.

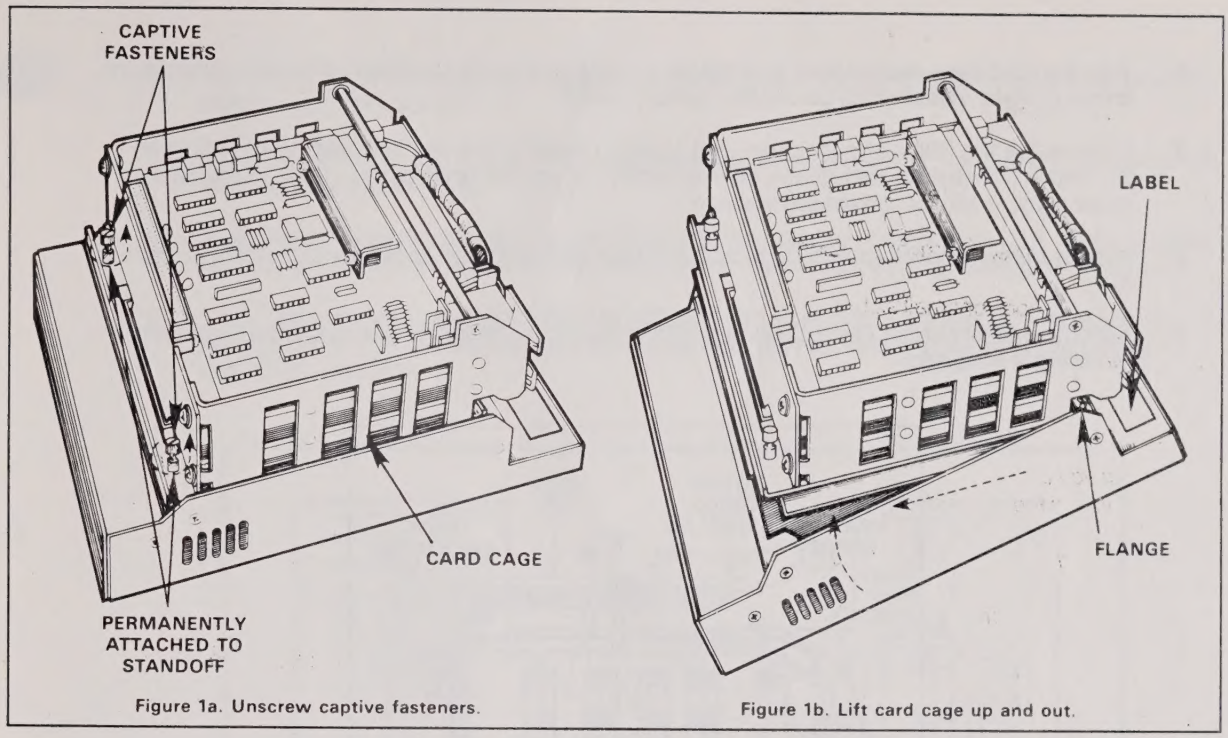

Figure 1a. Unscrew captive fasteners.

Figure 1b. Lift card cage up and out.

Figure 1. UniPak 2/2B Disassembly

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (figure 2). Do not detach the socketboard interconnect cable.

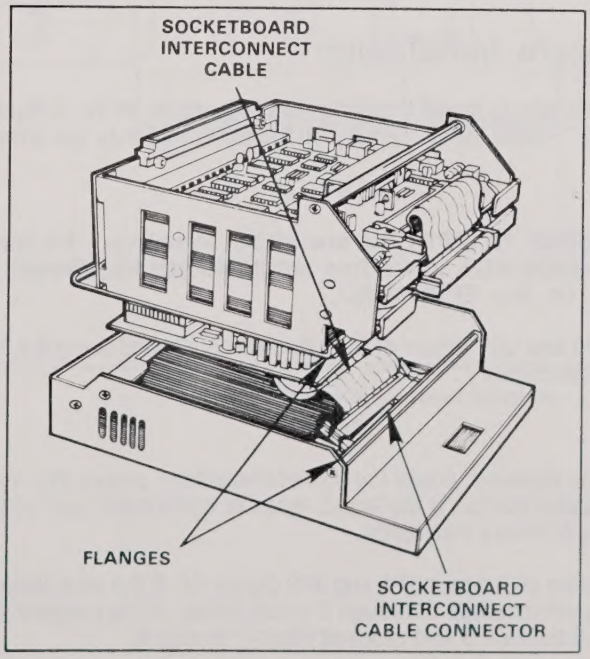

Figure 2. Socketboard Interconnect Cable

6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, it will not contain any washers.)

8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

9. Turn the memory board (figure 3) over so the component side faces up in preparation for update kit firmware installation.

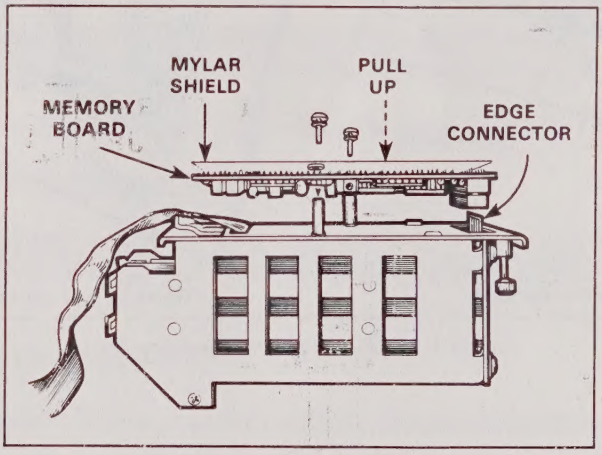

Figure 3. Memory Board Removal

Update Kit Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROM(s).

1. Remove EPROMs U20 and U21 (figure 4) from the memory board using the IC extractor tool or the small slot-head screwdriver.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

2. Observe the configuration of jumpers JP1 and JP2 (figure 4). If the wire strap jumpers are located in position B, perform steps 3 through 5 which follow. If the jumpers are located in position A, skip steps 3 through 5 and proceed directly to step 6.

3. If jumpers JP1 and JP2 are in position B, remove Decode PROM U19 (see figure 4 for location) using the IC extractor tool.

4. After removing Decode PROM U19, unsolder and switch jumpers JP1 and JP2 from position B, and resolder in position A.

5. Install the software update kit Decode PROM U19 in memory board socket U19. Refer to table 1 for software update kit firmware part numbers and their corresponding installation locations.

6. Install the software update kit EPROMs U20 and U21 in sockets U20 and U21, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

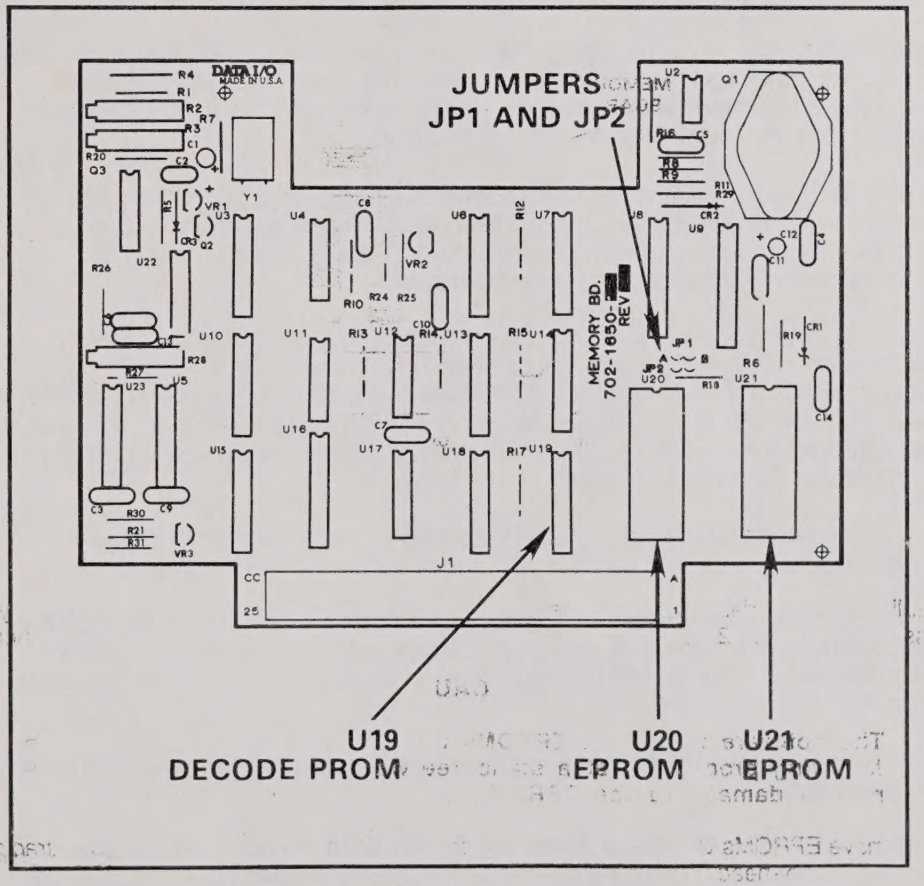

Figure 4. Update Component Location

DATA I/O

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